Datasheet | Rev. 4.0 | 2015

IMM2G64D3(L)DUD8AG (Die Revision B)
16GByte (2048M x 64 Bit)

16GB DDR3 Unbuffered DIMM
RoHS Compliant Product

Version: Rev. 4.0, JUN 2015

4.0 – Update the SPD information in Table 19
Update tRFC in Table 18

Version: Rev. 3.0, DEC 2014

3.0 – Revise the SPD information in Table 19

Version: Rev. 2.0, JUL 2014

2.0 – Updated CAS Latency support to include CL5
Added Operation temperature for Industrial Temperature Product in Table 10
Updated Input Switching Conditions in Table 13
Moved V_{SEH} information from Table 14 to Table 15
Updated IDD values in Table 17
Updated tAA, tRCD, tRRD, tRP, tFAW in Table 18, 19

Version: Rev. 1.0, NOV 2013

1.0 - Initial release

Remark:
Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures .

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Features

- 240-Pin Unbuffered Dual-In-Line Memory Module
- Capacity: 16GB
- JEDEC-Standard
- Bi-directional Differential Data-Strobe
- 64 Bit Data Bus Width without ECC
- Programmable CAS Latency (CL):
  - PC3-12800: 5, 6, 7, 8, 9, 10, 11
  - PC3-10600: 5, 6, 7, 8, 9, 10
- Programmable CAS Write Latency (CWL):
  - PC3-12800: 5, 6, 7, 8
  - PC3-10600: 5, 6, 7
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- On-Die Termination (ODT)
- ZQ Calibration Supported
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Asynchronous Reset
- Serial Presence Detect (SPD) with EEPROM
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 30.00mm (1.181 inch)

Table 1 - Ordering Information for RoHS Compliant Product				
Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM2G64D3xDUD8AG-Bzzzy	16GB	2Gx64	2	16GB DDR3 Unbuffered DIMM

Notes:
x: Operating Voltage
y: Operating Temperature
zzz: Speed Grade

Table 2 - Operating Voltage	
Part Number	Operating Voltage
Blank	VDD, VDDQ = 1.5V (1.425V-1.575V)
L	VDD, VDDQ = 1.35V (1.283V-1.45V) Backward compatible to VDD, VDDQ = 1.5V (1.425V-1.575V)

Table 3 - Temperature Grade		
Part Number	Temperature Grade	T_{case}
Blank	Commercial temperature	0°C to 95°C
I	Industrial temperature	-40°C to 95°C

Remark: Tcase is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85 °C < Tcase <= 95 °C.

Table 4 - Speed Grade		
Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
125	PC3-12800 (DDR3-1600)	800MHz (1.25ns@CL=11)
15E	PC3-10600 (DDR3-1333)	667MHz (1.5ns@CL=9)

Table 5 - Memory Chip Information					
Part Number	Base Device Brand	Base device	Voltage	Type	Chip Packing
IMM2G64D3LDUD8AG-Bzzzy	I'M	IM8G08D3FBBG	1.35V	1024Mx8	Lead Free
IMM2G64D3DUD8AG-Bzzzy	I'M	IM8G08D3EBBG	1.5V	1024Mx8	Lead Free

Part Number Decoder

IMM 2G64 D3 (L) DU D 8 A G - B 125 (I)

Intelligent Memory Module

Module Configuration
2G64 = 2Gx64 (16GB)

Memory Type
D3 = DDR3

DDR3L option
Blank = 1.5 Volt
L = 1.35 or 1.5 Volt (DDR3L)

Module Form-Factor
DU = Unbuffered DIMM

Number of Ranks
D = Dual Rank

DRAM Bit width
8 = using x8 components

Module PCB Revision
A = Revision A
B = Revision B
C = Revision C

RoHS compliance
G = Green / RoHS

IC Revision
A = Revision A
B = Revision B
C = Revision C

Speed Grade
15E = PC3-10600 / DDR3 1333
125 = PC3-12800 / DDR3 1600

Temperature Grade
Blank = Commercial Temperature (0°C to 95°C T_C)
I = Industrial Temperature (-40°C to 95°C T_C)

Table 6 - Addressing

Parameter	16GB
Refresh count	8K
Row address	64K A[15:0]
Device bank address	8 BA[2:0]
Device configuration	8Gb (1024Mx8)
Column address	2K A[9:0], A11
Module rank address	2 /S[1:0]
Number of devices	16

Table 7 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	121	VSS	61	A2	181	A1
2	VSS	122	D4	62	VDD	182	VDD
3	D0	123	D5	63	CK1	183	VDD
4	D1	124	VSS	64	/CK1	184	CK0
5	VSS	125	DM0	65	VDD	185	/CK0
6	/DQS0	126	NC	66	VDD	186	VDD
7	DQS0	127	VSS	67	VREFCA	187	NC
8	VSS	128	D6	68	NC	188	A0
9	D2	129	D7	69	VDD	189	VDD
10	D3	130	VSS	70	A10, AP	190	BA1
11	VSS	131	D12	71	BA0	191	VDD
12	D8	132	D13	72	VDD	192	/RAS
13	D9	133	VSS	73	/WE	193	/S0
14	VSS	134	DM1	74	/CAS	194	VDD
15	/DQS1	135	NC	75	VDD	195	ODT0
16	DQS1	136	VSS	76	/S1	196	A13
17	VSS	137	D14	77	ODT1	197	VDD
18	D10	138	D15	78	VDD	198	NC
19	D11	139	VSS	79	NC	199	VSS
20	VSS	140	D20	80	VSS	200	D36
21	D16	141	D21	81	D32	201	D37
22	D17	142	VSS	82	D33	202	VSS
23	VSS	143	DM2	83	VSS	203	DM4
24	/DQS2	144	NC	84	/DQS4	204	NC
25	DQS2	145	VSS	85	DQS4	205	VSS
26	VSS	146	D22	86	VSS	206	D38
27	D18	147	D23	87	D34	207	D39
28	D19	148	VSS	88	D35	208	VSS
29	VSS	149	D28	89	VSS	209	D44
30	D24	150	D29	90	D40	210	D45
31	D25	151	VSS	91	D41	211	VSS
32	VSS	152	DM3	92	VSS	212	DM5
33	/DQS3	153	NC	93	/DQS5	213	NC
34	DQS3	154	VSS	94	DQS5	214	VSS
35	VSS	155	D30	95	VSS	215	D46
36	D26	156	D31	96	D42	216	D47
37	D27	157	VSS	97	D43	217	VSS
38	VSS	158	NC	98	VSS	218	D52
39	NC	159	NC	99	D48	219	D53
40	NC	160	VSS	100	D49	220	VSS
41	VSS	161	NC	101	VSS	221	DM6
42	NC	162	NC	102	/DQS6	222	NC
43	NC	163	VSS	103	DQS6	223	VSS
44	VSS	164	NC	104	VSS	224	D54
45	NC	165	NC	105	D50	225	D55
46	NC	166	VSS	106	D51	226	VSS
47	VSS	167	NC	107	VSS	227	D60
48	NC	168	/RESET	108	D56	228	D61
49	NC	169	CKE1	109	D57	229	VSS
50	CKE0	170	VDD	110	VSS	230	DM7
51	VDD	171	A15	111	/DQS7	231	NC
52	BA2	172	A14	112	DQS7	232	VSS
53	NC	173	VDD	113	VSS	233	D62
54	VDD	174	A12, /BC	114	D58	234	D63
55	A11	175	A9	115	D59	235	VSS
56	A7	176	VDD	116	VSS	236	VDDSPD
57	VDD	177	A8	117	SA0	237	SA1
58	A5	178	A6	118	SCL	238	SDA

Pin	Name	Pin	Name	Pin	Name	Pin	Name
59	A4	179	VDD	119	SA2	239	VSS
60	VDD	180	A3	120	VTT	240	VTT

Table 8 - Pin Description

Pin Name	Description	Pin Name	Description
VDD	SDRAM core power supply	VREFDQ	SDRAM I/O reference supply
VREFCA	SDRAM command/address reference supply	VSS	Power supply return (ground)
A0-A15	SDRAM address bus	BA0-BA2	SDRAM bank addresses
CK0-CK1	SDRAM clocks (positive line of differential pair)	/CK0-/CK1	SDRAM clocks (negative line of differential pair)
/RAS	SDRAM row address strobe	/CAS	SDRAM column address strobe
/WE	SDRAM write enable	CKE0-CKE1	SDRAM clock enable lines
/S0-/S1	DIMM Rank Select Lines	ODT0-ODT1	On-die termination control lines
DQS0-DQS7	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS7	SDRAM data strobes (negative line of differential pair)
D0-D63	DIMM memory data bus	DM0-DM7	SDRAM data mask/high data strobes
SCL	EEPROM clock	SDA	EEPROM date line
SA0-SA1	EEPROM address input	VDDSPD	EEPROM positive power supply
/RESET	Reset Pin	VTT	Termination Voltage
NC	Spare Pins (no connect)		

Figure 1 – Module Dimension 240 Pin DDR3 SDRAM Unbuffered DIMM

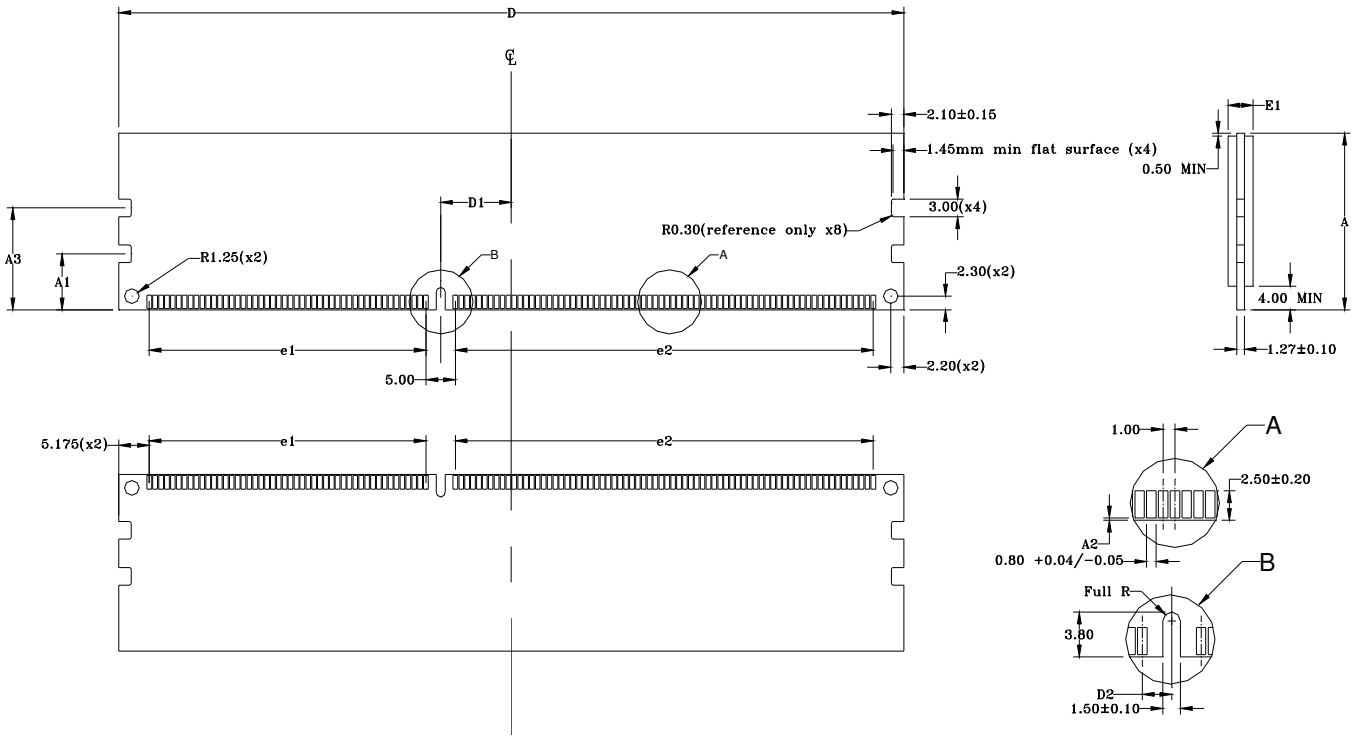


Table 9 - PCB Dimension			
Symbol	MIN	NOM	MAX
A	29.85	30.00	30.50
A1		9.35	
A2	0.05	0.20	0.35
A3	17.15	17.30	17.45
D	133.20	133.35	133.50
D1		12.00 Basic	
D2		2.50 Basic	
e1		47.00 Basic	
e2		71.00 Basic	
E1			4.00

Notes:

- All dimensioning and tolerancing conform to ASME Y14.5M-1994.
- Tolerances for all dimensions ±0.15 unless otherwise specified.
- All dimensions are in millimeters.

Figure 2 – Functional Block Diagram (Page 1 of 2)

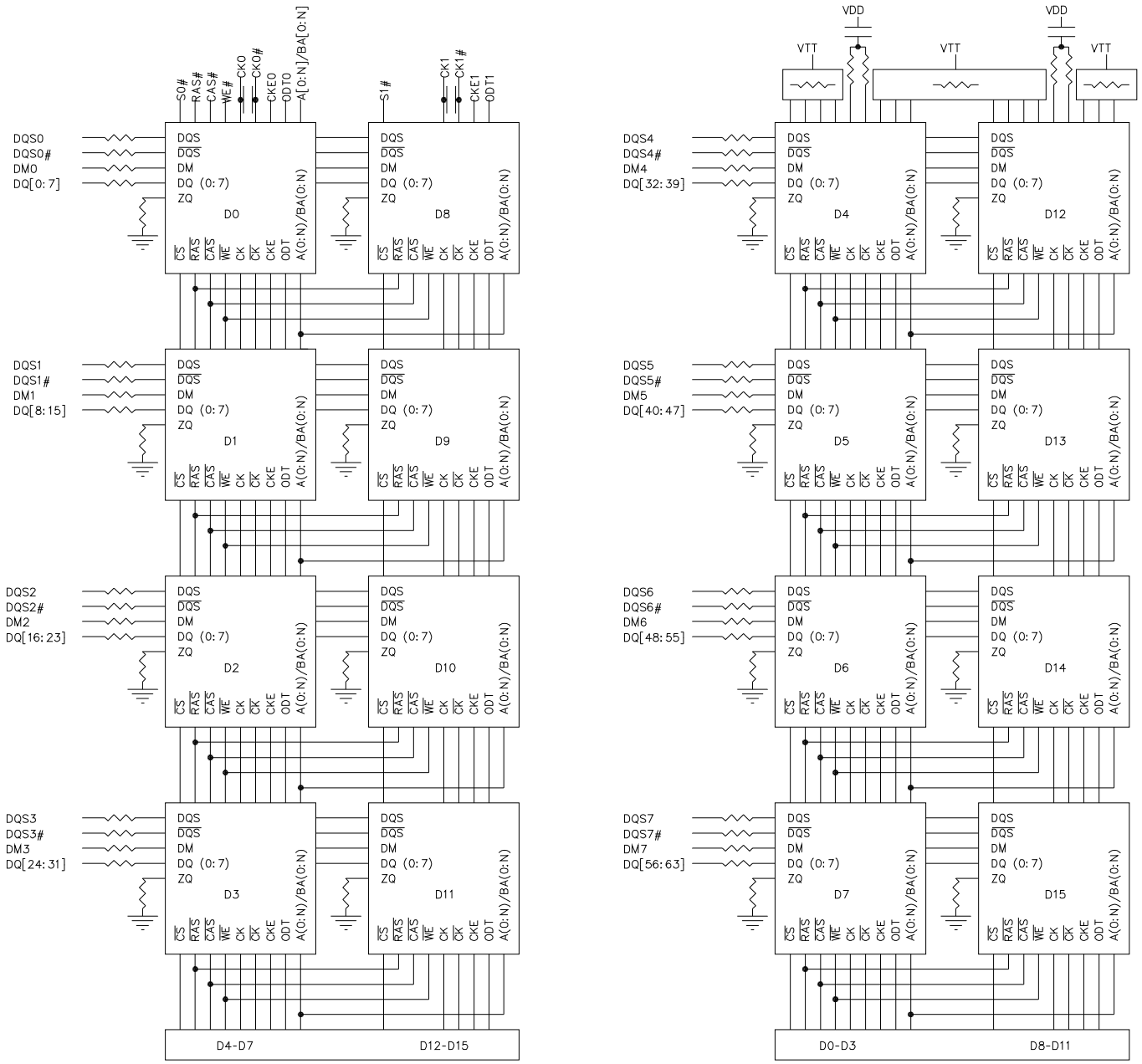
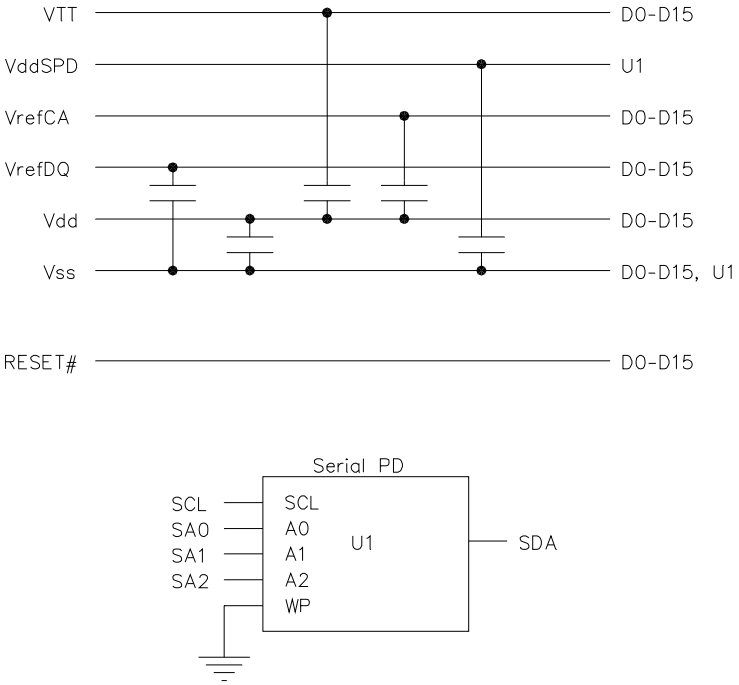


Figure 3 – Functional Block Diagram (Page 2 of 2)



Electrical Parameter

Table 10 - Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on V_{DD}, pin relative to V_{SS}	V_{DD}	-0.4V ~ 1.975	V	1,3
Voltage on V_{DDQ}, pin relative to V_{SS}	V_{DDQ}	-0.4V ~ 1.975	V	1,3
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	-0.4V ~ 1.975	V	1
DRAM Storage temperature	T_{STG}	-55 ~ 100	°C	1,2
DRAM Operation temperature (Standard Product)	Tcase	0 ~ 95	°C	2,4,6
DRAM Operation temperature (Industrial Temperature Product)	Tcase	-40 ~ 95	°C	2,5,6

Notes:

1 Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2 Storage Temperature or DRAM operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

3 VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6 x VDDQ, when VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

4 The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-95 °C under all operating conditions.

5 The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between -40-95 °C under all operating conditions.

6 Some applications require operation of the Extended Temperature Range between 85 °C and 95 °C case temperature. Full Specifications are guaranteed in this range but the following additional conditions apply
a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us.
b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

Table 11 - DC Electrical Characteristics and Operating Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ.	Max		
Supply voltage	V_{DD}	1.283	1.35	1.45	V	1,2
I/O supply voltage	V_{DDQ}				V	1,2
Supply voltage	V_{DD}	1.425	1.5	1.575	V	1,2,3
I/O supply voltage	V_{DDQ}				V	1,2,3

Notes:

1 VDD and VDDQ must track one another. VDDQ must be less than or equal to VDD. VSS = VSSQ.

2 VDD and VDDQ may include AC noise of +/-50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. VDD and VDDQ must be at same level for valid AC timing parameters.

3 Module is backward-compatible with 1.5V operation.

Table 12 - DC Electrical Characteristics and Input Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ.	Max		
V_{IN} low; DC/commands/address buses (1.35V Operation)	V_{IL}	V_{SS}	-	-0.090	V	
V_{IN} low; DC/commands/address buses (1.5V Operation)	V_{IL}	V_{SS}	-	-0.100	V	
V_{IN} high; DC/commands/address buses (1.35V Operation)	V_{IH}	0.090	-	V_{DD}	V	
V_{IN} high; DC/commands/address buses (1.5V Operation)	V_{IH}	0.100	-	V_{DD}	V	
Input reference voltage; command/address bus	$V_{REFCA(DC)}$	0.49* V_{DD}	0.50* V_{DD}	0.51* V_{DD}	V	1,2
I/O reference voltage DQ bus	$V_{REFDQ(DC)}$	0.49* V_{DD}	0.50* V_{DD}	0.51* V_{DD}	V	2,3
Command/address termination voltage (system level, not direct DRAM input)	V_{TT}	-	0.50* V_{DDQ}	-	V	4

Notes:

1. VREFCA(DC) is expected to be approximately 0.5 × VDD and to track variations in the DC level. Externally generated peak noise (noncommon mode) on VREFCA may not exceed ±1% × VDD around the VREFCA(DC) value. Peak-to-peak AC noise on VREFCA should not exceed ±2% of VREFCA(DC).
2. DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20 MHz in frequency.
3. VREFDQ(DC) is expected to be approximately 0.5 × VDD and to track variations in the DC level. Externally generated peak noise (noncommon mode) on VREFDQ may not exceed ±1% × VDD around the VREFDQ(DC) value. Peak-to-peak AC noise on VREFDQ should not exceed ±2% of VREFDQ(DC).
4. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors. MIN and MAX values are system-dependent.

Table 13 - Input Switching Conditions

Parameter / Condition	Symbol	Value		Units
		1.35V Operation	1.5V Operation	
Command and Address				
Input high AC voltage: Logic 1 @ 175mV	$V_{IH(AC175)min}$	-	175	mV
Input high AC voltage: Logic 1 @ 160mV	$V_{IH(AC160)min}$	160	-	mV
Input high AC voltage: Logic 1 @ 150mV	$V_{IH(AC150)min}$	-	150	mV
Input high AC voltage: Logic 1 @ 135mV	$V_{IH(AC135)min}$	135	-	mV
Input high DC voltage: Logic 1 @ 100mV	$V_{IH(DC100)min}$	-	100	mV
Input high DC voltage: Logic 1 @ 90mV	$V_{IH(DC90)min}$	90	-	mV
Input low DC voltage: Logic 0 @ -90mV	$V_{IL(DC90)max}$	-90	-	mV
Input low DC voltage: Logic 0 @ -100mV	$V_{IL(DC100)max}$	-	-100	mV
Input low AC voltage: Logic 0 @ -135mV	$V_{IL(AC135)max}$	-135	-	mV
Input low AC voltage: Logic 0 @ -150mV	$V_{IL(AC150)max}$	-	-150	mV
Input low AC voltage: Logic 0 @ -160mV	$V_{IL(AC160)max}$	-160	-	mV
Input low AC voltage: Logic 0 @ -175mV	$V_{IL(AC175)max}$	-	-175	mV
DQ and DM				
Input high AC voltage: Logic 1	$V_{IH(AC150)min}$	-	150	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}$	135	-	mV
Input high DC voltage: Logic 1	$V_{IH(DC100)min}$	-	100	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	-	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)max}$	-90	-	mV
Input low DC voltage: Logic 0	$V_{IL(DC100)max}$	-	-100	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)max}$	-135	-	mV
Input low AC voltage: Logic 0	$V_{IL(AC150)max}$	-	-150	mV

Notes:

1 All voltages are referenced to VREF. VREF is VREFCA for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. VREF is VREFDQ for DQ and DM inputs.

2 Input setup timing parameters (tIS and tDS) are referenced at VIL(AC)/VIH(AC), not VREF(DC).

3 Input hold timing parameters (tIH and tDH) are referenced at VIL(DC)/VIH(DC), not VREF(DC).

4 Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).

Table 14 - Differential Input Operating Conditions (CK, /CK and DQS, /DQS)

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Differential input voltage logic high – slew (1.35V Operation)	$V_{IH,diff}$	+180	-	mV	1
Differential input voltage logic high – slew (1.5V Operation)	$V_{IH,diff}$	+200	-	mV	1
Differential input voltage logic low – slew (1.35V Operation)	$V_{IL,diff}$	-	-180	mV	1
Differential input voltage logic low – slew (1.5V Operation)	$V_{IL,diff}$	-	-200	mV	1
Differential input voltage logic high	$V_{IH,diff(AC)}$	2* (VIH(AC) - VREF)	-	mV	2
Differential input voltage logic low	$V_{IL,diff(AC)}$	-	2* (VIL(AC) - VREF)	mV	3
Differential Input Cross Point Voltage relative to VDD/2 for CK, CK (1.35V Operation)	V_{IX}	-150	150	mV	4
Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS (1.35V Operation)	V_{IX}	-150	150	mV	
Differential Input Cross Point Voltage relative to VDD/2 for CK, CK (1.5V Operation)	V_{IX}	-150	150	mV	
		-175	175		5
Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS (1.5V Operation)	V_{IX}	-150	150	mV	

Notes:

1 Defines slew rate reference points, relative to input crossing voltages.

2 Minimum DC limit is relative to single-ended signals; overshoot specifications are applicable.

3 Maximum DC limit is relative to single-ended signals; undershoot specifications are applicable.

4 The relation between V_{IX} Min/Max and V_{SEL}/V_{SEH} should satisfy following:
$(V_{DD}/2) + V_{IX(min)} - V_{SEL} >= 25mV$;
$V_{SEH} - ((V_{DD}/2) + V_{IX(max)}) >= 25mV$;

5 Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and /CK are monotonic with a single-ended swing V_{SEL}/V_{SEH} of at least $V_{DD}/2$ +/-250mV, and when the differential slew rate of CK-/CK is larger than 3V/ns.

Table 15 - Single-Ended Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{REF} - 0.1 * V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.1 * V_{DDQ}$ (1.35V Operation)	SRQse	1.75	5	V/ns	1,2,3
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{REF} - 0.1 * V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.1 * V_{DDQ}$ (1.5V Operation)	SRQse	2.5	5	V/ns	1,2,3
Single-ended high level for strobes	V_{SEH}	VDDQ/2 + 175	-	mV	2
Single-ended high level for CK, /CK		VDD/2 + 175	-	mV	2
Single-ended low level for strobes	V_{SEL}	-	VDDQ/2 - 175	mV	3
Single-ended low level for CK, /CK		-	VDD/2 - 175	mV	3
Single-ended DC high-level output voltage	$V_{OH(DC)}$	$0.8 * V_{DDQ}$		V	1
Single-ended DC mid-level output voltage	$V_{OM(DC)}$	$0.5 * V_{DDQ}$		V	1
Single-ended DC low-level output voltage	$V_{OL(DC)}$	$0.2 * V_{DDQ}$		V	1
Single-ended AC high-level output voltage	$V_{OH(AC)}$	$V_{TT} + 0.1 * V_{DDQ}$		V	1,2
Single-ended AC low-level output voltage	$V_{OL(AC)}$	$V_{TT} - 0.1 * V_{DDQ}$		V	1,2
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				

Notes:

1 RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (VDDQ = VDD, VSSQ = VSS).

2 VTT = VDDQ/2.

3 The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or all switching the opposite direction. For all other DQ signal switching combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.

Table 16 - Differential Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)}$ = -0.2 * V_{DDQ} and $V_{OH,diff(AC)}$ = + 0.2 * V_{DDQ} (1.35V Operation)	SRQ_{diff}	3.5	12	V/ns	1
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)}$ = -0.2 * V_{DDQ} and $V_{OH,diff(AC)}$ = + 0.2 * V_{DDQ} (1.5V Operation)	SRQ_{diff}	5	10	V/ns	1
Differential high-level output voltage	$V_{OH,diff(AC)}$	+0.2 * V_{DDQ}		V	1
Differential low-level output voltage	$V_{OL,diff(AC)}$	-0.2 * V_{DDQ}		V	1
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				

Notes:

1 RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (VDDQ = VDD, VSSQ = VSS).

2 VREF = VDDQ/2; slew rate @ 5V/ns, interpolate for faster slew rate.

For part number IMM2G64D3(L)DUD8AG-B125(I)

Table 17 - IDD Specifications with Conditions and Operation Current

Parameter / Condition	Symbol	Current		Units	Notes
		1.35V Operation	1.5V Operation		
Operating current 0; One bank ACTIVATE-to-PRECHARGE	I_{DD0}	1008	1080	mA	1, 2
Operating current 1; One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	1264	1360	mA	1, 2
Precharge power-down current; Slow exit	I_{DD2P0}	448	480	mA	1, 3
Precharge power-down current; Fast exit	I_{DD2P1}	448	480	mA	1, 3
Precharge quiet standby current	I_{DD2Q}	576	640	mA	1, 3
Precharge standby current	I_{DD2N}	896	960	mA	1, 3
Precharge standby ODT current	I_{DD2NT}	1056	1120	mA	1, 3
Active power-down current	I_{DD3P}	480	512	mA	1, 3
Active standby current	I_{DD3N}	992	1120	mA	1, 3
Burst read operating current	I_{DD4R}	2424	2560	mA	1, 2
Burst write operating current	I_{DD4W}	1344	1440	mA	1, 2
Refresh current	I_{DD5B}	2664	2800	mA	1, 2
Self refresh temperature current: MAX T_c = 85°C	I_{DD6}	320	352	mA	1, 3
Self refresh temperature current (SRT-enabled): MAX T_c = 95°C	I_{DD6ET}	320	352	mA	1, 3
All banks interleaved read current	I_{DD7}	3464	3640	mA	1, 2
Reset current	I_{DD8}	368	400	mA	1, 2

Notes:

1 Value shown for DDR3 SDRAM only and are computed from values specified in the 8Gbit component data sheet.

2 One module rank in the active IDD, the other rank in IDD2P0.

3 All ranks in this IDD conditions.

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Table 18 - AC Timing Parameter and Operating Conditions

Parameter / Condition		Symbol	Min	Max	Units
Clock Timing					
Clock period average: DLL disable mode	T_C = 0°C to 85°C	tCK (DLL_DIS)	8	7800	ns
	T_C => 85°C to 95°C		8	3900	
Clock periods average: DLL enable mode (CL = 11, CWL = 8)		tCK (AVG)	1.25	<1.5	ns
Clock periods average: DLL enable mode (CL = 9, CWL = 7)		tCK (AVG)	1.5	<1.875	ns
High pulse width average		tCH (AVG)	0.47	0.53	tCK
Low pulse width average		tCL (AVG)	0.47	0.53	tCK
Clock period jitter	DLL locked	tJITper	-70	70	ps
	DLL locking	tJITper,lck	-60	60	ps
Clock absolute period		tCK (ABS)	tCK (AVG) MIN + tJITper MIN	tCK (AVG) MAX + tJITper MAX	ps
Clock absolute high pulse width		tCH (ABS)	0.43	-	tCK (AVG)
Clock absolute low pulse width		tCL (ABS)	0.43	-	tCK (AVG)
Cycle-to-cycle jitter	DLL locked	tJITcc	-	140	ps
	DLL locking	tJITcc,lck	-	120	ps
Cumulative error across	2 cycles	tERR2per	-103	103	ps
	3 cycles	tERR3per	-122	122	ps
	4 cycles	tERR4per	-136	136	ps
	5 cycles	tERR5per	-147	147	ps
	6 cycles	tERR6per	-155	155	ps
	7 cycles	tERR7per	-163	163	ps
	8 cycles	tERR8per	-169	169	ps
	9 cycles	tERR9per	-175	175	ps
	10 cycles	tERR10per	-180	180	ps
	11 cycles	tERR11per	-184	184	ps
	12 cycles	tERR12per	-188	188	ps
	n = 14,…49, 50 cycles	tERRnper	(1+0.68ln[n]) * tJITper MIN	(1+0.68ln[n]) * tJITper Max	ps
DQ Input Timing					
Data setup time to DQS, /DQS (1.35V Operation)	Base (specification)	tDS (AC135)	25	-	ps
					ps
Data setup time to DQS, /DQS (1.5V Operation)	Base (specification)	tDS (AC150)	10	-	ps
					ps
Data hold time from DQS, /DQS (1.35V Operation)	Base (specification)	tDH (DC90)	55	-	ps
					ps
Data hold time from DQS, /DQS (1.5V Operation)	Base (specification)	tDH (DC100)	45	-	ps
					ps
Minimum data pulse width		tDIPW	360	-	ps
DQ Output Timing					
DQS, /DQS to DQ skew, per access		tDQSQ	-	100	ps
DQ output hold time from DQS, /DQS		tQH	0.38	-	tCK (AVG)
DQ Low-Z time from CK, /CK		tLZDQ	-450	225	ps
DQ High-Z time from CK, /CK		tHZDQ	-	225	ps
DQ Strobe Input Timing					
DQS, /DQS rising to CK, /CK rising		tDQSS	-0.27	0.27	tCK
DQS, /DQS differential input low pulse width		tDQSL	0.45	0.55	tCK

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Parameter / Condition		Symbol	Min	Max	Units
DQS, /DQS falling setup to CK, /CK rising		tDSS	0.18	-	tCK
DQS, /DQS falling hold from CK, /CK rising		tDSH	0.18	-	tCK
DQS, /DQS differential input high pulse width		tDQSH	0.45	0.55	tCK
DQS, /DQS differential WRITE preamble		tWPRE	0.9	-	tCK
DQS, /DQS differential WRITE postamble		tWPST	0.3	-	tCK
DQ Strobe Output Timing					
DQS, /DQS rising to/from CK, /CK		tDQSCK	-225	225	ps
DQS, /DQS differential output high time		tQSH	0.40	-	tCK
DQS, /DQS differential output low time		tQSL	0.40	-	tCK
DQS, /DQS Low-Z time (RL-1)		tLZDQS	-450	225	ps
DQS, /DQS High-Z time (RL+BL/2)		tHZDQS	-	225	ps
DQS, /DQS differential READ preamble		tRPRE	0.9	greater of tLZ(DQS) (MIN), tDQSK (MAX)	tCK
DQS, /DQS differential READ postamble		tRPST	0.3	greater of tDQSCK (MIN) + tQSH (MIN), tHZ(DQS) (MAX)	tCK
Command and Address Timing					
DLL locking time		tDLLK	512	-	tCK
CTRL, CMD, ADDR setup to CK, /CK (1.35V Operation)	Base (specification)	tIS (AC160)	60	-	ps
CTRL, CMD, ADDR setup to CK, /CK (1.5V Operation)	Base (specification)	tIS (AC175)	45	-	ps
CTRL, CMD, ADDR setup to CK, /CK (1.35V Operation)	Base (specification)	tIS (AC135)	185	-	ps
CTRL, CMD, ADDR setup to CK, /CK (1.5V Operation)	Base (specification)	tIS (AC150)	170	-	ps
CTRL, CMD, ADDR hold from CK, /CK (1.35V Operation)	Base (specification)	tIH (DC90)	130	-	ps
CTRL, CMD, ADDR hold from CK, /CK (1.5V Operation)	Base (specification)	tIH (DC100)	120	-	ps
Minimum CTRL, CMD, ADDR pulse width		tIPW	560	-	ps
ACTIVATE to internal READ or WRITE delay		tRCD	13.125	-	ns
PRECHARGE command period		tRP	13.125	-	ns
ACTIVATE-to-PRECHARGE command period		tRAS	35	9 * tREFI	ns
ACTIVATE-to-ACTIVATE command period		tRC	48.125	-	ns
ACTIVATE-to-ACTIVATE minimum period		tRRD	greater of 4tCK or 7.5ns	-	tCK
Four ACTIVATE windows (2KB page size)		tFAW	40	-	ns
Write recovery time		tWR	15	-	ns
Delay from start of internal WRITE transaction to internal READ command		tWTR	greater of 4tCK or 7.5ns	-	tCK
READ-to-PRECHARGE time		tRTP	greater of 4tCK or 7.5ns	-	tCK
/CAS-to-/CAS command delay		tCCD	4	-	tCK
Auto precharge write recovery + precharge time		tDAL	WR + tRP/ tCK (AVG)	-	tCK
MODE REGISTER SET command cycle time		tMRD	4	-	tCK
MODE REGISTER SET command update delay		tMOD	greater of 12tCK or 15ns	-	tCK
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		tMPRR	1	-	tCK
Calibration Timing					
ZQCL command: Long calibration time	POWER-UP and RESET operation	tZQinit	greater of 512 tCK	-	tCK
	Normal operation	tZQoper	greater of 256 tCK	-	tCK
ZQCS command: Short calibration time		tZQcs	greater of 64 tCK	-	tCK

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Parameter / Condition		Symbol	Min	Max	Units
Initialization and Reset Timing					
Exit reset from CKE HIGH to valid command		^{t}XPR	greater of 5^{t}CK or ^{t}RFC(min)+10ns	-	^{t}CK
Refresh Timing					
REFRESH-to-ACTIVATE or REFRESH command period		^{t}RFC	300	-	ns
Maximum refresh period	Tc<=85oC	-	64 (1X)		ms
	Tc>85oC		32 (2X)		
Maximum average periodic refresh	Tc<=85oC	^{t}REFI	7.8 (64ms/8192)		us
	Tc>85oC		3.9 (32ms/8192)		
Self Refresh Timing					
Exit self refresh to commands not requiring a locked DLL		^{t}XS	greater of 5 ^{t}CK or ^{t}RFC+10ns	-	^{t}CK
Exit self refresh to commands requiring a locked DLL		^{t}XSDLL	^{t}DLLK (MIN)	-	^{t}CK
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		^{t}CKESR	^{t}CKE (MIN) + ^{t}CK	-	^{t}CK
Valid clocks after self refresh entry or power down entry		^{t}CKSRE	greater of 5^{t}CK or 10ns	-	^{t}CK
Valid clocks before self refresh exit, power-down exit, or reset exit		^{t}CKSRX	greater of 5^{t}CK or 10ns	-	^{t}CK
Power-Down Timing					
CKE MIN pulse width		^{t}CKE (MIN)	greater of 3^{t}CK or 5ns		^{t}CK
Command pass disable delay		^{t}CPDED	1	-	^{t}CK
Power-down entry to power exit timing		^{t}PD	^{t}CKE (MIN)	9 * ^{t}REFI	^{t}CK
Power-Down Entry Minimum Timing					
ACTIVATE command to power-down entry		^{t}ACTPDEN	1	-	^{t}CK
PRECHARGE/PRECHARGE ALL command to power-down entry		^{t}PRPDEN	1	-	^{t}CK
REFRESH command to power-down entry		^{t}REFPDEN	1	-	^{t}CK
MRS command to power-down entry		^{t}MRSPDEN	MIN = ^{t}MOD (MIN)		^{t}CK
READ/READ with auto precharge command to power-down entry		^{t}RDPDEN	MIN = RL + 4 + 1		^{t}CK
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRPDEN	MIN = WL + 4 + ^{t}WR/tCK (AVG)		^{t}CK
	BC4MRS	^{t}WRPDEN	MIN = WL + 2 + ^{t}WR/^{t}CK (AVG)		^{t}CK
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRAPDEN	MIN = WL + 4 + ^{t}WR + 1		^{t}CK
	BC4MRS	^{t}WRAPDEN	MIN = WL + 2 + ^{t}WR + 1		^{t}CK
Power-Down Exit Timing					
DLL on, any valid command, or DLL off to commands not requiring locked DLL		^{t}XP	greater of 3^{t}CK or 6ns	-	^{t}CK
Precharge power-down with DLL off to commands requiring a locked DLL		^{t}XPDLL	greater of 10^{t}CK or 24ns	--	^{t}CK
ODT Timing					
R_{TT} turn-on from ODTL on reference		^{t}AON	-225	225	ps
R_{TT} turn-off from ODTL off reference		^{t}AOF	0.3	0.7	^{t}CK (AVG)
Asynchronous R_{TT} turn-on delay (power-down with DLL off)		^{t}AONPD	2	8.5	ns
Asynchronous RTT turn-off delay (power-down with DLL off)		^{t}AOFPD	2	8.5	ns
ODT high time without write command or with write command and BC4		ODTH4	4	-	tCK
ODT high time with Write command and BL8		ODTH8	6	-	tCK

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Parameter / Condition	Symbol	Min	Max	Units
Dynamic ODT Timing				
R_{TT} dynamic change skew	^{t}ADC	0.3	0.7	^{t}CK (AVG)
Write Leveling Timing				
First DQS, /DQS rising edge	^{t}WLMRD	40	-	^{t}CK
DQS, /DQS delay	^{t}WLDQSEN	25	-	^{t}CK
Write leveling setup from rising CK, /CK crossing to rising DQS, /DQS crossing	^{t}WLS	165	-	ps
Write leveling hold from rising DQS, /DQS crossing to rising CK, /CK crossing	$_{t}$WLH	165	-	ps
Write leveling output delay	^{t}WLO	0	7.5	ns
Write leveling output error	^{t}WLOE	0	2	ns

For part number IMM2G64D3(L)DUD8AG-B125(I)

Table 19 – SPD Information

Byte NO.	Description	Note		Hex	
		1.35V Operation	1.5V Operation	1.35V Operation	1.5V Operation
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	176 / 256 / 0-116		92	
1	SPD Revision	1.2		12	
2	Key Byte / DRAM Device Type	DDR3 SDRAM		0B	
3	Key Byte / Module Type	Regular Unbuffered DIMM		02	
4	SDRAM Density and Banks	8Gb 8banks		05	
5	SDRAM Addressing	Row 16 / Col 11		22	
6	Module Nominal Voltage, VDD	1.35V/1.5V	1.5V	02	00
7	Module Organization	2Rank , x8		09	
8	Module Memory Bus Width	Non-ECC, 64bit		03	
9	Fine Timebase (FTB) Dividend and Divisor	2.5ps		52	
10	Medium Timebase (MTB) Dividend	1/8 (0.125ns)		01	
11	Medium Timebase (MTB) Divisor	1/8 (0.125ns)		08	
12	SDRAM Minimum Cycle Time (tCKmin)	1.25ns		0A	
13	Reserved	-		00	
14	CAS Latencies Supported, Least Significant Byte	5, 6, 7, 8, 9, 10, 11		FE	
15	CAS Latencies Supported, Most Significant Byte	-		00	
16	Minimum CAS Latency Time (tAAmin)	13.125ns		69	
17	Minimum Write Recovery Time (tWRmin)	15ns		78	
18	Minimum /RAS to /CAS Delay Time (tRCDmin)	13.125ns		69	
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	7.5ns		3C	
20	Minimum Row Precharge Time (tRPmin)	13.125ns		69	
21	Upper Nibbles for tRAS and tRC	-		11	
22	Minimum Active to Precharge Time (tRASmin), LSB	35ns		18	
23	Minimum Active to Active/Refresh Time (tRCmin), LSB	48.125ns		81	
24	Minimum Refresh Recovery Time (tRFCmin), LSB	300ns		60	
25	Minimum Refresh Recovery Time (tRFCmin), MSB	300ns		09	
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	7.5ns		3C	
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns		3C	
28	Upper Nibble for tFAW	40ns		01	
29	Minimum Four Activate Window Delay Time (tFAWmin), LSB	40ns		40	
30	SDRAM Optional Features	DLL off Mode, RZQ/6, RZQ/7		83	
31	SDRAM Thermal and Refresh Options	0-95°C Op. Temp. w/2x refresh		05	
32	Module Thermal Sensor	Without TS		00	
33	SDRAM Device Type	Non-Standard SDRAM		A1	
34-59	Reserved, General Section	-		00	
60	Module Nominal Height	29< Height <= 30		0F	

Byte NO.	Description	Note	Hex	
61	Module Maximum Thickness	1< Tf <=2 (mm); 1< Tb <=2 (mm)	11	
62	Reference Raw Card Used	Raw Card B1	21	
63	Address Mapping from Edge Connector to DRAM	Mirror Mapping	01	
64-116	Module Type Specific Section, Indexed by Key Byte	-	00	
117-118	Module ID: Module Manufacturer's JEDEC ID Code	Reserved	Reserved	
119	Module ID: Module Manufacturing Location	Reserved	Reserved	
120-121	Module ID: Module Manufacturing Date	Reserved	Reserved	
122-125	Module ID: Module Serial Number	Reserved	Reserved	
126-127	Cyclical Redundancy Code	-	57 BB	FC 3C
128-145	Module Part Number	Reserved	Reserved	
146-147	Module Revision Code	Reserved	Reserved	
148-149	DRAM Manufacturer's JEDEC ID Code	Reserved	Reserved	
150-175	Manufacturer's Specific Data	Reserved	Reserved	
176-255	Open For Customer Use	Reserved	Reserved	

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