

Datasheet | Rev. 5.0 | 2015

IMM2G64D3(L)SOD8AG (Die Revision B) 16GByte (2048M x 64 Bit)

16GB DDR3 Unbuffered SO-DIMM
RoHS Compliant Product

Version: Rev. 5.0, JUN 2015

- 5.0 – Update the SPD information in Table 19
- Update tRFC in Table 18

Version: Rev. 4.0, JAN 2015

- 4.0 – Added DRAM operation temperature for Industrial Temperature Product in Table 10.
- Updated notes in Table 12, 13
- Moved V_{SEH} information from Table 14 to Table 15
- Corrected tCPDED in Table 18

Version: Rev. 3.0, JUN 2014

- 3.0 – Added module thickness E in Table 9

Version: Rev. 2.0, MAY 2014

- 2.0 – Updated CAS Latency support to include CL5
- Updated IDD values in Table 17
- Updated tAA, tRCD, tRRD, tRP, tFAW in Table 18, 19

Version: Rev. 1.0, NOV 2013

- 1.0 - Initial release

Remark:

Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures .

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Features

- 204-Pin Unbuffered Small Outline Dual-In-Line Memory Module
- Capacity: 16GB
- JEDEC-Standard
- Bi-directional Differential Data-Strobe
- 64 Bit Data Bus Width without ECC
- Programmable CAS Latency (CL):
 - PC3-12800: 5, 6, 7, 8, 9, 10, 11
 - PC3-10600: 5, 6, 7, 8, 9, 10
- Programmable CAS Write Latency (CWL):
 - PC3-12800: 5, 6, 7, 8
 - PC3-10600: 5, 6, 7
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- On-Die Termination (ODT)
- ZQ Calibration Supported
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Asynchronous Reset
- Serial Presence Detect (SPD) with EEPROM
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 30.00mm (1.181 inch)

Table 1 - Ordering Information for RoHS Compliant Product

Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM2G64D3xSOD8AG-Bzzzy	16GB	2Gx64	2	16GB DDR3 Unbuffered SO-DIMM

Notes:

x: Operating Voltage
y: Operating Temperature
zzz: Speed Grade

Table 2 - Operating Voltage

Part Number	Operating Voltage
Blank	VDD, VDDQ = 1.5V (1.425V-1.575V)
L	VDD, VDDQ = 1.35V (1.283V-1.45V) Backward compatible to VDD, VDDQ = 1.5V (1.425V-1.575V)

Table 3 - Temperature Grade

Part Number	Temperature Grade	T _{case}
Blank	Commercial temperature	0°C to 95°C
I	Industrial temperature	-40°C to 95°C

Remark: T_{case} is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85 °C < T_{case} ≤ 95 °C.

Table 4 - Speed Grade

Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
125	PC3-12800 (DDR3-1600)	800MHz (1.25ns@CL=11)
15E	PC3-10600 (DDR3-1333)	667MHz (1.5ns@CL=9)

Table 5 - Memory Chip Information

Part Number	Base Device Brand	Base device	Voltage	Type	Chip Packing
IMM2G64D3LSOD8AG-Bzzzy	I'M	IM8G08D3FBGG	1.35V	1024Mx8	Lead Free
IMM2G64D3SOD8AG-Bzzzy	I'M	IM8G08D3EBGG	1.5V	1024Mx8	Lead Free

Part Number Decoder

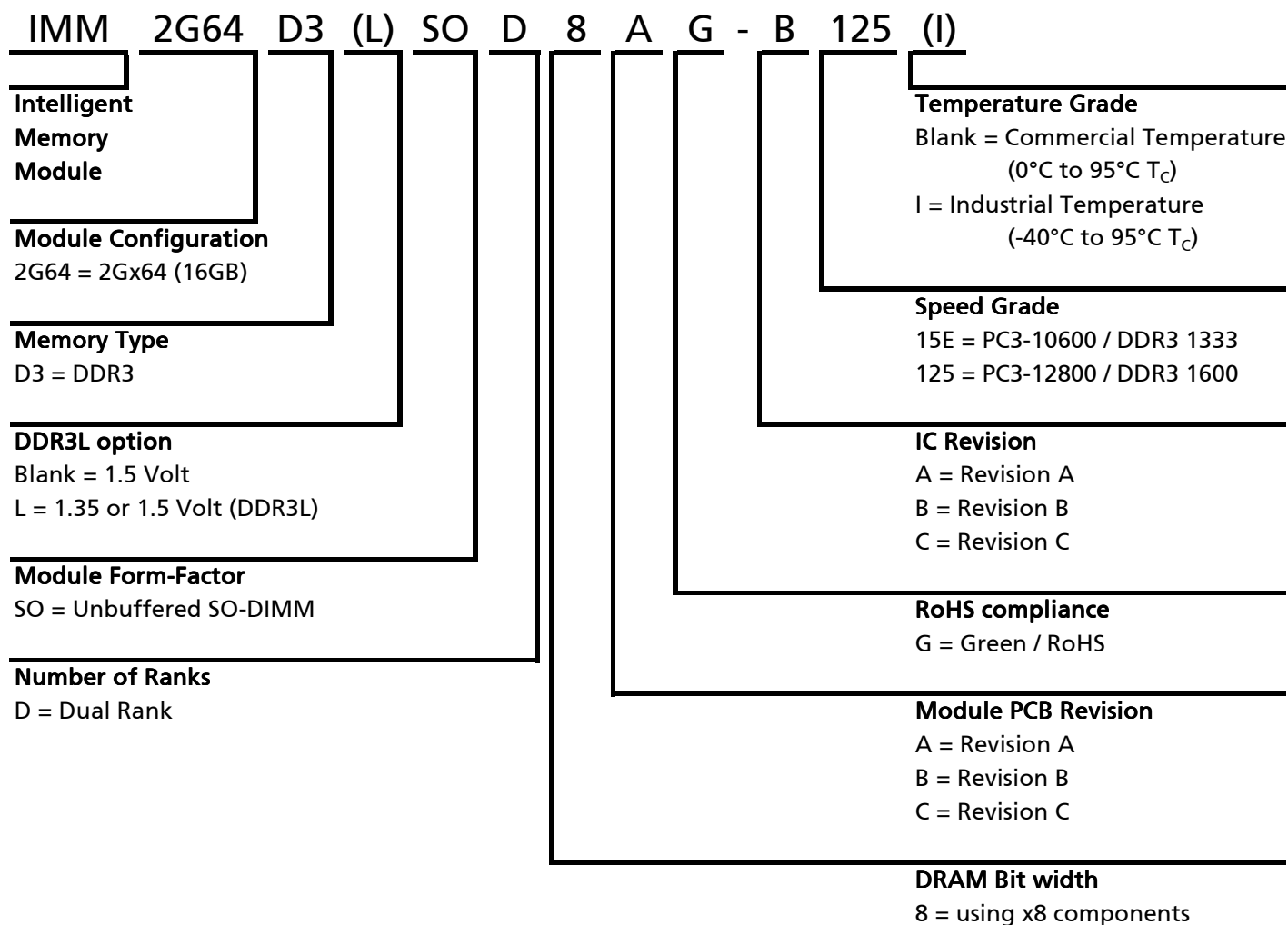


Table 6 - Addressing

Parameter	16GB
Refresh count	8K
Row address	64K A[15:0]
Device bank address	8 BA[2:0]
Device configuration	8Gb (1024Mx8)
Column address	2K A[9:0], A11
Module rank address	2 /S[1:0]
Number of devices	16

Table 7 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	2	VSS	103	/CK0	104	/CK1
3	VSS	4	D4	105	VDD	106	VDD
5	D0	6	D5	107	A10, AP	108	BA1
7	D1	8	VSS	109	BA0	110	/RAS
9	VSS	10	/DQS0	111	VDD	112	VDD
11	DM0	12	DQS0	113	/WE	114	/S0
13	VSS	14	VSS	115	/CAS	116	ODT0
15	D2	16	D6	117	VDD	118	VDD
17	D3	18	D7	119	A13	120	ODT1
19	VSS	20	VSS	121	/S1	122	NC
21	D8	22	D12	123	VDD	124	VDD
23	D9	24	D13	125	NC	126	VREFCA
25	VSS	26	VSS	127	VSS	128	VSS
27	/DQS1	28	DM1	129	D32	130	D36
29	DQS1	30	/RESET	131	D33	132	D37
31	VSS	32	VSS	133	VSS	134	VSS
33	D10	34	D14	135	/DQS4	136	DM4
35	D11	36	D15	137	DQS4	138	VSS
37	VSS	38	VSS	139	VSS	140	D38
39	D16	40	D20	141	D34	142	D39
41	D17	42	D21	143	D35	144	VSS
43	VSS	44	VSS	145	VSS	146	D44
45	/DQS2	46	DM2	147	D40	148	D45
47	DQS2	48	VSS	149	D41	150	VSS
49	VSS	50	D22	151	VSS	152	/DQS5
51	D18	52	D23	153	DM5	154	DQS5
53	D19	54	VSS	155	VSS	156	VSS
55	VSS	56	D28	157	D42	158	D46
57	D24	58	D29	159	D43	160	D47
59	D25	60	VSS	161	VSS	162	VSS
61	VSS	62	/DQS3	163	D48	164	D52
63	DM3	64	DQS3	165	D49	166	D53
65	VSS	66	VSS	167	VSS	168	VSS
67	D26	68	D30	169	/DQS6	170	DM6
69	D27	70	D31	171	DQS6	172	VSS
71	VSS	72	VSS	173	VSS	174	D54
73	CKE0	74	CKE1	175	D50	176	D55
75	VDD	76	VDD	177	D51	178	VSS
77	NC	78	A15	179	VSS	180	D60
79	BA2	80	A14	181	D56	182	D61
81	VDD	82	VDD	183	D57	184	VSS
83	A12,/BC	84	A11	185	VSS	186	/DQS7
85	A9	86	A7	187	DM7	188	DQS7
87	VDD	88	VDD	189	VSS	190	VSS
89	A8	90	A6	191	D58	192	D62
91	A5	92	A4	193	D59	194	D63
93	VDD	94	VDD	195	VSS	196	VSS
95	A3	96	A2	197	SA0	198	NC
97	A1	98	A0	199	VDDSPD	200	SDA
99	VDD	100	VDD	201	SA1	202	SCL
101	CK0	102	CK1	203	VTI	204	VTI

Table 8 - Pin Description

Pin Name	Description	Pin Name	Description
VDD	SDRAM core power supply	VREFDQ	SDRAM I/O reference supply
VREFCA	SDRAM command/address reference supply	VSS	Power supply return (ground)
A0-A15	SDRAM address bus	BA0-BA2	SDRAM bank addresses
CK0-CK1	SDRAM clocks (positive line of differential pair)	/CK0-/CK1	SDRAM clocks (negative line of differential pair)
/RAS	SDRAM row address strobe	/CAS	SDRAM column address strobe
/WE	SDRAM write enable	CKE0-CKE1	SDRAM clock enable lines
/S0-/S1	DIMM Rank Select Lines	ODT0-ODT1	On-die termination control lines
DQS0-DQS7	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS7	SDRAM data strobes (negative line of differential pair)
D0-D63	DIMM memory data bus	DM0-DM7	SDRAM data mask/high data strobes
SCL	EEPROM clock	SDA	EEPROM data line
SA0-SA1	EEPROM address input	VDDSPD	EEPROM positive power supply
/RESET	Reset Pin	VTT	Termination Voltage
NC	Spare Pins (no connect)		

Figure 1 – Module Dimension 204 Pin DDR3 SDRAM Unbuffered SO-DIMM

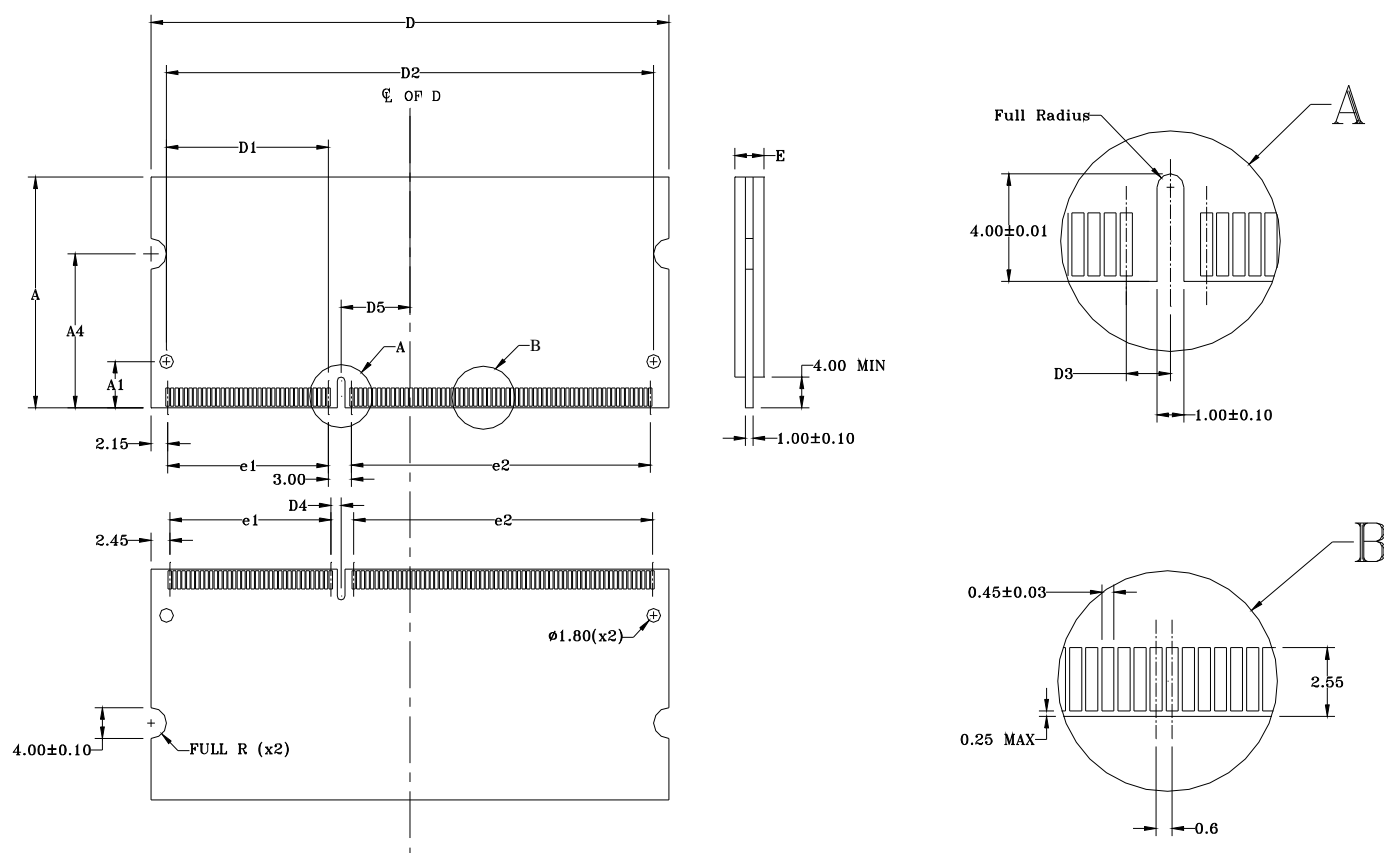


Table 9 - PCB Dimension

Symbol	MIN	NOM	MAX
A	29.85	30.00	30.15
A1	20.00 Basic		
D	67.45	67.60	67.75
D2	63.60 Basic		
D3	1.65 Basic		
D5	9.00 Basic		
e1	21.00 Basic		
e2	39.00 Basic		
E			3.80

Notes:

- All dimensioning and tolerancing conform to ASME Y14.5M-1994.
- Tolerances for all dimensions ± 0.15 unless otherwise specified.
- All dimensions are in millimeters.

Figure 2 – Functional Block Diagram (Page 1 of 2)

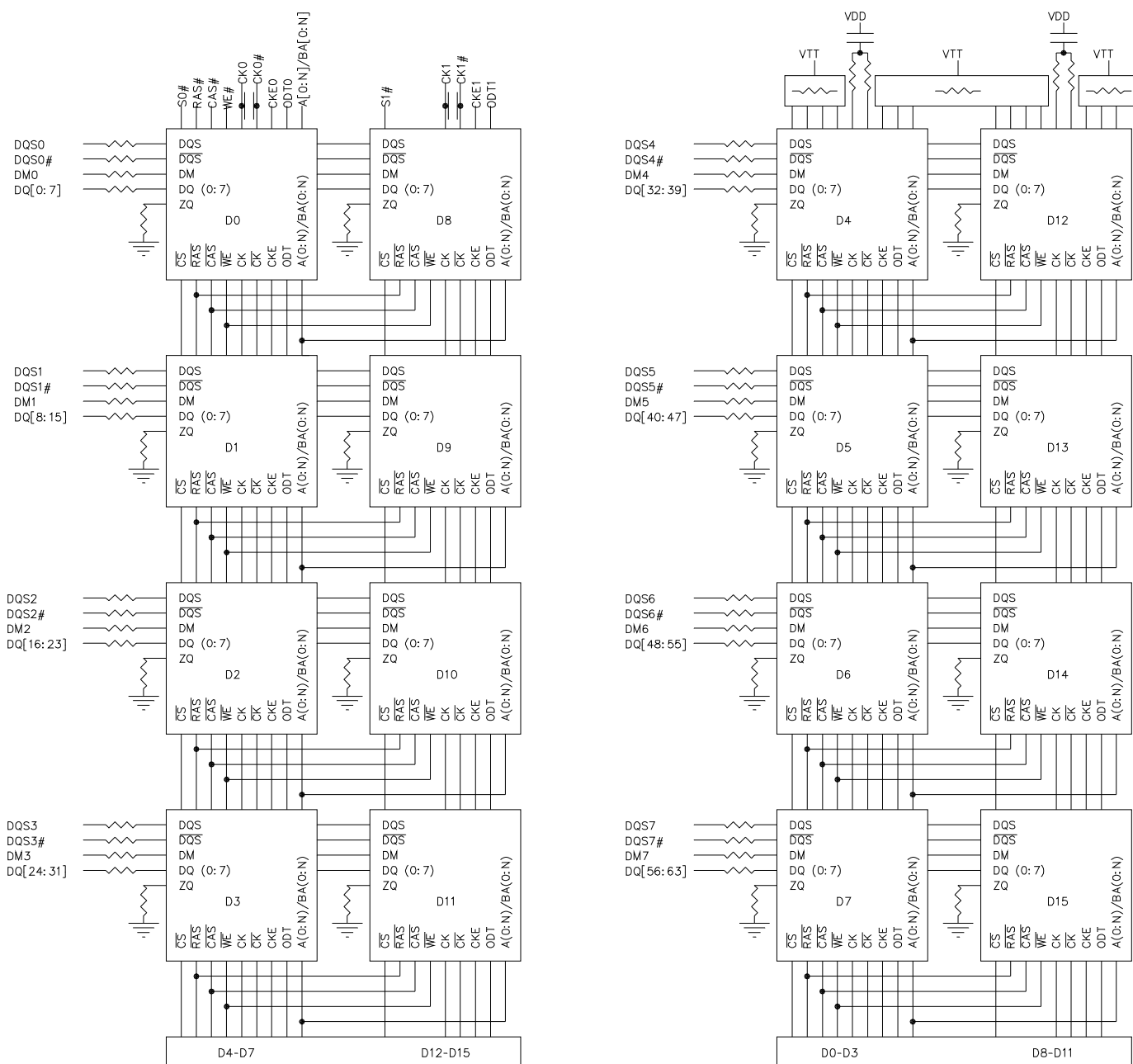
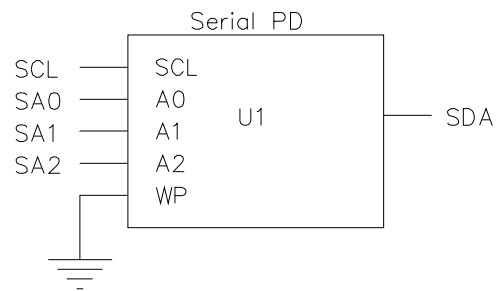
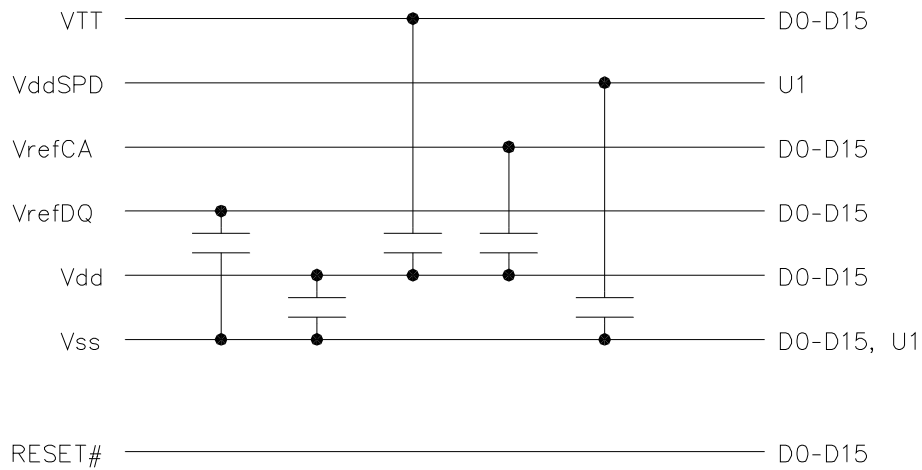


Figure 3 – Functional Block Diagram (Page 2 of 2)



Electrical Parameter

Table 10 - Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on V_{DD} , pin relative to V_{SS}	V_{DD}	-0.4V ~ 1.975	V	1,3
Voltage on V_{DDQ} , pin relative to V_{SS}	V_{DDQ}	-0.4V ~ 1.975	V	1,3
Voltage on any pins relative to V_{SS}	V_{IN} , V_{OUT}	-0.4V ~ 1.975	V	1
DRAM Storage temperature	T_{STG}	-55 ~ 100	°C	1,2
DRAM Operation temperature (Standard Product)	T_{case}	0 ~ 95	°C	2,4,6
DRAM Operation temperature (Industrial Temperature Product)	T_{case}	-40 ~ 95	°C	2,5,6

Notes:

- ¹ Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- ² Storage Temperature or DRAM operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- ³ VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6 x VDDQ, when VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.
- ⁴ The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-95 °C under all operating conditions.
- ⁵ The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between -40-95 °C under all operating conditions.
- ⁶ Some applications require operation of the Extended Temperature Range between 85 °C and 95 °C case temperature. Full Specifications are guaranteed in this range but the following additional conditions apply
 - a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us.
 - b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

Table 11 - DC Electrical Characteristics and Operating Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ.	Max		
Supply voltage	V_{DD}	1.283	1.35	1.45	V	1,2
I/O supply voltage	V_{DDQ}				V	1,2
Supply voltage	V_{DD}	1.425	1.5	1.575	V	1,2,3
I/O supply voltage	V_{DDQ}				V	1,2,3

Notes:

- ¹ VDD and VDDQ must track one another. VDDQ must be less than or equal to VDD. VSS = VSSQ.
- ² VDD and VDDQ may include AC noise of +/-50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. VDD and VDDQ must be at same level for valid AC timing parameters.
- ³ Module is backward-compatible with 1.5V operation.

Table 12 - DC Electrical Characteristics and Input Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ.	Max		
V_{IN} low; DC/commands/address buses (1.35V Operation)	V_{IL}	V_{SS}	-	-0.090	V	
V_{IN} low; DC/commands/address buses (1.5V Operation)	V_{IL}	V_{SS}	-	-0.100	V	
V_{IN} high; DC/commands/address buses (1.35V Operation)	V_{IH}	0.090	-	V_{DD}	V	
V_{IN} high; DC/commands/address buses (1.5V Operation)	V_{IH}	0.100	-	V_{DD}	V	
Input reference voltage; command/address bus	$V_{REFCA(DC)}$	$0.49 \times V_{DD}$	$0.50 \times V_{DD}$	$0.51 \times V_{DD}$	V	1,2
I/O reference voltage DQ bus	$V_{REFDQ(DC)}$	$0.49 \times V_{DD}$	$0.50 \times V_{DD}$	$0.51 \times V_{DD}$	V	2,3
Command/address termination voltage (system level, not direct DRAM input)	V_{TT}	-	$0.50 \times V_{DDQ}$	-	V	4

Notes:

- ¹ $V_{REFCA(DC)}$ is expected to be approximately $0.5 \times V_{DD}$ and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFCA} may not exceed $\pm 1\% \times V_{DD}$ around the $V_{REFCA(DC)}$ value. Peak-to-peak AC noise on V_{REFCA} should not exceed $\pm 2\%$ of $V_{REFCA(DC)}$.
- ² DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20 MHz in frequency.
- ³ $V_{REFDQ(DC)}$ is expected to be approximately $0.5 \times V_{DD}$ and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFDQ} may not exceed $\pm 1\% \times V_{DD}$ around the $V_{REFDQ(DC)}$ value. Peak-to-peak AC noise on V_{REFDQ} should not exceed $\pm 2\%$ of $V_{REFDQ(DC)}$.
- ⁴ V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors. MIN and MAX values are system-dependent.

Table 13 - Input Switching Conditions

Parameter / Condition	Symbol	Value		Units
		1.35V Operation	1.5V Operation	
Command and Address				
Input high AC voltage: Logic 1 @ 175mV	$V_{IH(AC175)min}$	-	175	mV
Input high AC voltage: Logic 1 @ 160mV	$V_{IH(AC160)min}$	160	-	mV
Input high AC voltage: Logic 1 @ 150mV	$V_{IH(AC150)min}$	-	150	mV
Input high AC voltage: Logic 1 @ 135mV	$V_{IH(AC135)min}$	135	-	mV
Input high DC voltage: Logic 1 @ 100mV	$V_{IH(DC100)min}$	-	100	mV
Input high DC voltage: Logic 1 @ 90mV	$V_{IH(DC90)min}$	90	-	mV
Input low DC voltage: Logic 0 @ -90mV	$V_{IL(DC90)max}$	-90	-	mV
Input low DC voltage: Logic 0 @ -100mV	$V_{IL(DC100)max}$	-	-100	mV
Input low AC voltage: Logic 0 @ -135mV	$V_{IL(AC135)max}$	-135	-	mV
Input low AC voltage: Logic 0 @ -150mV	$V_{IL(AC150)max}$	-	-150	mV
Input low AC voltage: Logic 0 @ -160mV	$V_{IL(AC160)max}$	-160	-	mV
Input low AC voltage: Logic 0 @ -175mV	$V_{IL(AC175)max}$	-	-175	mV
DQ and DM				
Input high AC voltage: Logic 1	$V_{IH(AC150)min}$	-	150	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}$	135	-	mV
Input high DC voltage: Logic 1	$V_{IH(DC100)min}$	-	100	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	-	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)max}$	-90	-	mV
Input low DC voltage: Logic 0	$V_{IL(DC100)max}$	-	-100	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)max}$	-135	-	mV
Input low AC voltage: Logic 0	$V_{IL(AC150)max}$	-	-150	mV

Notes:

- ¹ All voltages are referenced to VREF. VREF is VREFCA for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. VREF is VREFDQ for DQ and DM inputs.
- ² Input setup timing parameters (tIS and tDS) are referenced at $V_{IL(AC)}/V_{IH(AC)}$, not $V_{REF(DC)}$.
- ³ Input hold timing parameters (tIH and tDH) are referenced at $V_{IL(DC)}/V_{IH(DC)}$, not $V_{REF(DC)}$.
- ⁴ Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).

Table 14 - Differential Input Operating Conditions (CK, /CK and DQS, /DQS)

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Differential input voltage logic high – slew (1.35V Operation)	$V_{IH,diff}$	+180	-	mV	1
Differential input voltage logic high – slew (1.5V Operation)	$V_{IH,diff}$	+200	-	mV	1
Differential input voltage logic low – slew (1.35V Operation)	$V_{IL,diff}$	-	-180	mV	1
Differential input voltage logic low – slew (1.5V Operation)	$V_{IL,diff}$	-	-200	mV	1
Differential input voltage logic high	$V_{IH,diff(AC)}$	$2 * (V_{IH(AC)} - V_{REF})$	-	mV	2
Differential input voltage logic low	$V_{IL,diff(AC)}$	-	$2 * (V_{IL(AC)} - V_{REF})$	mV	3
Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK, /CK (1.35V Operation)	V_{IX}	-150	150	mV	4
Differential Input Cross Point Voltage relative to $V_{DD}/2$ for DQS, /DQS (1.35V Operation)	V_{IX}	-150	150	mV	
Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK, /CK (1.5V Operation)	V_{IX}	-150	150	mV	5
		-175	175		
Differential Input Cross Point Voltage relative to $V_{DD}/2$ for DQS, /DQS (1.5V Operation)	V_{IX}	-150	150	mV	

Notes:

- 1 Defines slew rate reference points, relative to input crossing voltages.
- 2 Minimum DC limit is relative to single-ended signals; overshoot specifications are applicable.
- 3 Maximum DC limit is relative to single-ended signals; undershoot specifications are applicable.
- 4 The relation between V_{IX} Min/Max and V_{SEL}/V_{SEH} should satisfy following:
 $(V_{DD}/2) + V_{IX(min)} - V_{SEL} \geq 25mV$;
 $V_{SEH} - ((V_{DD}/2) + V_{IX(max)}) \geq 25mV$;
- 5 Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and /CK are monotonic with a single-ended swing V_{SEL}/V_{SEH} of at least $V_{DD}/2 \pm 250mV$, and when the differential slew rate of CK-/CK is larger than 3V/ns.

Table 15 - Single-Ended Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{REF} - 0.1 * V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.1 * V_{DDQ}$ (1.35V Operation)	SRQse	1.75	5	V/ns	1,2,3
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{REF} - 0.1 * V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.1 * V_{DDQ}$ (1.5V Operation)	SRQse	2.5	5	V/ns	1,2,3
Single-ended high level for strobes	V_{SEH}	$V_{DDQ}/2 + 175$	-	mV	2
Single-ended high level for CK, /CK		$V_{DD}/2 + 175$	-	mV	2
Single-ended low level for strobes	V_{SEL}	-	$V_{DDQ}/2 - 175$	mV	3
Single-ended low level for CK, /CK		-	$V_{DD}/2 - 175$	mV	3
Single-ended DC high-level output voltage	$V_{OH(DC)}$	$0.8 * V_{DDQ}$		V	1
Single-ended DC mid-level output voltage	$V_{OM(DC)}$	$0.5 * V_{DDQ}$		V	1
Single-ended DC low-level output voltage	$V_{OL(DC)}$	$0.2 * V_{DDQ}$		V	1
Single-ended AC high-level output voltage	$V_{OH(AC)}$	$V_{TT} + 0.1 * V_{DDQ}$		V	1,2
Single-ended AC low-level output voltage	$V_{OL(AC)}$	$V_{TT} - 0.1 * V_{DDQ}$		V	1,2
Test load for AC timing and output slew rates	Output to V_{TT} ($V_{DDQ}/2$) via 25Ω resistor				

Notes:

- ¹ RZQ of 240Ω ($\pm 1\%$) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$, $V_{SSQ} = V_{SS}$).
- ² $V_{TT} = V_{DDQ}/2$.
- ³ The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or all switching the opposite direction. For all other DQ signal switching combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.

Table 16 - Differential Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)} = -0.2 * V_{DDQ}$ and $V_{OH,diff(AC)} = +0.2 * V_{DDQ}$ (1.35V Operation)	SRQ_{diff}	3.5	12	V/ns	1
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)} = -0.2 * V_{DDQ}$ and $V_{OH,diff(AC)} = +0.2 * V_{DDQ}$ (1.5V Operation)	SRQ_{diff}	5	10	V/ns	1
Differential high-level output voltage	$V_{OH,diff(AC)}$	$+0.2 * V_{DDQ}$		V	1
Differential low-level output voltage	$V_{OL,diff(AC)}$	$-0.2 * V_{DDQ}$		V	1
Test load for AC timing and output slew rates	Output to V_{TT} ($V_{DDQ}/2$) via 25Ω resistor				

Notes:

- ¹ RZQ of 240Ω ($\pm 1\%$) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$, $V_{SSQ} = V_{SS}$).
- ² $V_{REF} = V_{DDQ}/2$; slew rate @ 5V/ns, interpolate for faster slew rate.

For part number IMM2G64D3(L)SOD8AG-B125(I)

Table 17 - IDD Specifications with Conditions and Operation Current

Parameter / Condition	Symbol	Current		Units	Notes
		1.35V Operation	1.5V Operation		
Operating current 0; One bank ACTIVATE-to-PRECHARGE	I_{DD0}	1008	1080	mA	1, 2
Operating current 1; One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	1264	1360	mA	1, 2
Precharge power-down current; Slow exit	I_{DD2P0}	448	480	mA	1, 3
Precharge power-down current; Fast exit	I_{DD2P1}	448	480	mA	1, 3
Precharge quiet standby current	I_{DD2Q}	576	640	mA	1, 3
Precharge standby current	I_{DD2N}	896	960	mA	1, 3
Precharge standby ODT current	I_{DD2NT}	1056	1120	mA	1, 3
Active power-down current	I_{DD3P}	480	512	mA	1, 3
Active standby current	I_{DD3N}	992	1120	mA	1, 3
Burst read operating current	I_{DD4R}	2424	2560	mA	1, 2
Burst write operating current	I_{DD4W}	1344	1440	mA	1, 2
Refresh current	I_{DD5B}	2664	2800	mA	1, 2
Self refresh temperature current: MAX $T_c = 85^\circ\text{C}$	I_{DD6}	320	352	mA	1, 3
Self refresh temperature current (SRT-enabled): MAX $T_c = 95^\circ\text{C}$	I_{DD6ET}	320	352	mA	1, 3
All banks interleaved read current	I_{DD7}	3464	3640	mA	1, 2
Reset current	I_{DD8}	368	400	mA	1, 2

Notes:

- ¹ Value shown for DDR3 SDRAM only and are computed from values specified in the 8Gbit component data sheet.
- ² One module rank in the active IDD, the other rank in IDD2P0.
- ³ All ranks in this IDD conditions.

For part number IMM2G64D3(L)SOD8AG-B125(I)

Table 18 - AC Timing Parameter and Operating Conditions

Parameter / Condition		Symbol	Min	Max	Units
Clock Timing					
Clock period average: DLL disable mode	$T_C = 0^{\circ}\text{C to } 85^{\circ}\text{C}$	$t_{CK}(\text{DLL_DIS})$	8	7800	ns
	$T_C \Rightarrow 85^{\circ}\text{C to } 95^{\circ}\text{C}$		8	3900	
Clock periods average: DLL enable mode (CL = 11, CWL = 8)		$t_{CK}(\text{AVG})$	1.25	<1.5	ns
Clock periods average: DLL enable mode (CL = 9, CWL = 7)		$t_{CK}(\text{AVG})$	1.5	<1.875	ns
High pulse width average		$t_{CH}(\text{AVG})$	0.47	0.53	t_{CK}
Low pulse width average		$t_{CL}(\text{AVG})$	0.47	0.53	t_{CK}
Clock period jitter	DLL locked	t_{JITper}	-70	70	ps
	DLL locking	$t_{JITper,lck}$	-60	60	ps
Clock absolute period		$t_{CK}(\text{ABS})$	$t_{CK}(\text{AVG}) \text{ MIN} + t_{JITper}$	$t_{CK}(\text{AVG}) \text{ MAX} + t_{JITper}$	ps
Clock absolute high pulse width		$t_{CH}(\text{ABS})$	0.43	-	$t_{CK}(\text{AVG})$
Clock absolute low pulse width		$t_{CL}(\text{ABS})$	0.43	-	$t_{CK}(\text{AVG})$
Cycle-to-cycle jitter	DLL locked	t_{JITcc}	-	140	ps
	DLL locking	$t_{JITcc,lck}$	-	120	ps
Cumulative error across	2 cycles	$t_{ERR2per}$	-103	103	ps
	3 cycles	$t_{ERR3per}$	-122	122	ps
	4 cycles	$t_{ERR4per}$	-136	136	ps
	5 cycles	$t_{ERR5per}$	-147	147	ps
	6 cycles	$t_{ERR6per}$	-155	155	ps
	7 cycles	$t_{ERR7per}$	-163	163	ps
	8 cycles	$t_{ERR8per}$	-169	169	ps
	9 cycles	$t_{ERR9per}$	-175	175	ps
	10 cycles	$t_{ERR10per}$	-180	180	ps
	11 cycles	$t_{ERR11per}$	-184	184	ps
	12 cycles	$t_{ERR12per}$	-188	188	ps
	n = 14,...49, 50 cycles	$t_{ERRnper}$	$(1+0.68\ln[n]) * t_{JITper}$	$(1+0.68\ln[n]) * t_{JITper}$	ps
DQ Input Timing					
Data setup time to DQS, /DQS (1.35V Operation)	Base (specification)	$t_{DS}(\text{AC135})$	25	-	ps
					ps
Data setup time to DQS, /DQS (1.5V Operation)	Base (specification)	$t_{DS}(\text{AC150})$	10	-	ps
					ps
Data hold time from DQS, /DQS (1.35V Operation)	Base (specification)	$t_{DH}(\text{DC90})$	55	-	ps
					ps
Data hold time from DQS, /DQS (1.5V Operation)	Base (specification)	$t_{DH}(\text{DC100})$	45	-	ps
					ps
Minimum data pulse width		t_{DIPW}	360	-	ps
DQ Output Timing					
DQS, /DQS to DQ skew, per access		t_{DQSQ}	-	100	ps
DQ output hold time from DQS, /DQS		t_{QH}	0.38	-	$t_{CK}(\text{AVG})$
DQ Low-Z time from CK, /CK		t_{LZDQ}	-450	225	ps
DQ High-Z time from CK, /CK		t_{HZDQ}	-	225	ps
DQ Strobe Input Timing					
DQS, /DQS rising to CK, /CK rising		t_{DQSS}	-0.27	0.27	t_{CK}
DQS, /DQS differential input low pulse width		t_{DQSL}	0.45	0.55	t_{CK}

For part number IMM2G64D3(L)SOD8AG-B125(I)

Parameter / Condition		Symbol	Min	Max	Units
DQS, /DQS falling setup to CK, /CK rising		t_{DSS}	0.18	-	t_{CK}
DQS, /DQS falling hold from CK, /CK rising		t_{DSH}	0.18	-	t_{CK}
DQS, /DQS differential input high pulse width		t_{DQSH}	0.45	0.55	t_{CK}
DQS, /DQS differential WRITE preamble		t_{WPRE}	0.9	-	t_{CK}
DQS, /DQS differential WRITE postamble		t_{WPST}	0.3	-	t_{CK}
DQ Strobe Output Timing					
DQS, /DQS rising to/from CK, /CK		t_{DQSK}	-225	225	ps
DQS, /DQS differential output high time		t_{QSH}	0.40	-	t_{CK}
DQS, /DQS differential output low time		t_{QSL}	0.40	-	t_{CK}
DQS, /DQS Low-Z time (RL-1)		t_{LZDQS}	-450	225	ps
DQS, /DQS High-Z time (RL+BL/2)		t_{HZDQS}	-	225	ps
DQS, /DQS differential READ preamble		t_{RPRE}	0.9	greater of $t_{LZ(DQS)}$ (MIN), t_{DQSK} (MAX)	t_{CK}
DQS, /DQS differential READ postamble		t_{RPST}	0.3	greater of t_{DQSK} (MIN) + t_{QSH} (MIN), $t_{HZ(DQS)}$ (MAX)	t_{CK}
Command and Address Timing					
DLL locking time		t_{DLLK}	512	-	t_{CK}
CTRL, CMD, ADDR setup to CK, /CK (1.35V Operation)	Base (specification)	t_{IS} (AC160)	60	-	ps
CTRL, CMD, ADDR setup to CK, /CK (1.5V Operation)	Base (specification)	t_{IS} (AC175)	45	-	ps
CTRL, CMD, ADDR setup to CK, /CK (1.35V Operation)	Base (specification)	t_{IS} (AC135)	185	-	ps
CTRL, CMD, ADDR setup to CK, /CK (1.5V Operation)	Base (specification)	t_{IS} (AC150)	170	-	ps
CTRL, CMD, ADDR hold from CK, /CK (1.35V Operation)	Base (specification)	t_{IH} (DC90)	130	-	ps
CTRL, CMD, ADDR hold from CK, /CK (1.5V Operation)	Base (specification)	t_{IH} (DC100)	120	-	ps
Minimum CTRL, CMD, ADDR pulse width		t_{IPW}	560	-	ps
ACTIVATE to internal READ or WRITE delay		t_{RCD}	13.125	-	ns
PRECHARGE command period		t_{RP}	13.125	-	ns
ACTIVATE-to-PRECHARGE command period		t_{RAS}	35	$9 * t_{REFI}$	ns
ACTIVATE-to-ACTIVATE command period		t_{RC}	48.125	-	ns
ACTIVATE-to-ACTIVATE minimum period		t_{RRD}	greater of $4t_{CK}$ or 7.5ns	-	t_{CK}
Four ACTIVATE windows (2KB page size)		t_{FAW}	40	-	ns
Write recovery time		t_{WR}	15	-	ns
Delay from start of internal WRITE transaction to internal READ command		t_{WTR}	greater of $4t_{CK}$ or 7.5ns	-	t_{CK}
READ-to-PRECHARGE time		t_{RTP}	greater of $4t_{CK}$ or 7.5ns	-	t_{CK}
/CAS-to-/CAS command delay		t_{CCD}	4	-	t_{CK}
Auto precharge write recovery + precharge time		t_{DAL}	$WR + t_{RP} / t_{CK}$ (AVG)	-	t_{CK}
MODE REGISTER SET command cycle time		t_{MRD}	4	-	t_{CK}
MODE REGISTER SET command update delay		t_{MOD}	greater of $12t_{CK}$ or 15ns	-	t_{CK}
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		t_{MPRR}	1	-	t_{CK}
Calibration Timing					
ZQCL command: Long calibration time	POWER-UP and RESET operation	t_{ZQinit}	greater of $512 t_{CK}$	-	t_{CK}
	Normal operation	t_{ZQoper}	greater of $256 t_{CK}$	-	t_{CK}
ZQCS command: Short calibration time		t_{ZQcs}	greater of $64 t_{CK}$	-	t_{CK}

For part number IMM2G64D3(L)SOD8AG-B125(I)

Parameter / Condition		Symbol	Min	Max	Units
Initialization and Reset Timing					
Exit reset from CKE HIGH to valid command		^t XPR	greater of 5 ^t CK or ^t RFC(min)+10ns	-	^t CK
Refresh Timing					
REFRESH-to-ACTIVATE or REFRESH command period		^t RFC	300	-	ns
Maximum refresh period	Tc<=85oC	-	64 (1X)		ms
	Tc>85oC		32 (2X)		
Maximum average periodic refresh	Tc<=85oC	^t REFI	7.8 (64ms/8192)		us
	Tc>85oC		3.9 (32ms/8192)		
Self Refresh Timing					
Exit self refresh to commands not requiring a locked DLL		^t XS	greater of 5 ^t CK or ^t RFC+10ns	-	^t CK
Exit self refresh to commands requiring a locked DLL		^t XSDLL	^t DLLK (MIN)	-	^t CK
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		^t CKESR	^t CKE (MIN) + ^t CK	-	^t CK
Valid clocks after self refresh entry or power down entry		^t CKSRE	greater of 5 ^t CK or 10ns	-	^t CK
Valid clocks before self refresh exit, power-down exit, or reset exit		^t CKSRX	greater of 5 ^t CK or 10ns	-	^t CK
Power-Down Timing					
CKE MIN pulse width		^t CKE (MIN)	greater of 3 ^t CK or 5ns		^t CK
Command pass disable delay		^t CPDED	1	-	^t CK
Power-down entry to power exit timing		^t PD	^t CKE (MIN)	9 * ^t REFI	^t CK
Power-Down Entry Minimum Timing					
ACTIVATE command to power-down entry		^t ACTPDEN	1	-	^t CK
PRECHARGE/PRECHARGE ALL command to power-down entry		^t PRPDEN	1	-	^t CK
REFRESH command to power-down entry		^t REFPDEN	1	-	^t CK
MRS command to power-down entry		^t MRSPDEN	MIN = ^t MOD (MIN)		^t CK
READ/READ with auto precharge command to power-down entry		^t RDPDEN	MIN = RL + 4 + 1		^t CK
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	^t WRPDEN	MIN = WL + 4 + ^t WR/ ^t CK (AVG)		^t CK
	BC4MRS	^t WRPDEN	MIN = WL + 2 + ^t WR/ ^t CK (AVG)		^t CK
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	^t WRAPDEN	MIN = WL + 4 + ^t WR + 1		^t CK
	BC4MRS	^t WRAPDEN	MIN = WL + 2 + ^t WR + 1		^t CK
Power-Down Exit Timing					
DLL on, any valid command, or DLL off to commands not requiring locked DLL		^t XP	greater of 3 ^t CK or 6ns	-	^t CK
Precharge power-down with DLL off to commands requiring a locked DLL		^t XPDLL	greater of 10 ^t CK or 24ns	--	^t CK
ODT Timing					
R _{TT} turn-on from ODTL on reference		^t AON	-225	225	ps
R _{TT} turn-off from ODTL off reference		^t AOF	0.3	0.7	^t CK (AVG)
Asynchronous R _{TT} turn-on delay (power-down with DLL off)		^t AONPD	2	8.5	ns
Asynchronous R _{TT} turn-off delay (power-down with DLL off)		^t AOFPD	2	8.5	ns
ODT high time without write command or with write command and BC4		ODTH4	4	-	tCK
ODT high time with Write command and BL8		ODTH8	6	-	tCK

For part number IMM2G64D3(L)SOD8AG-B125(I)

Parameter / Condition	Symbol	Min	Max	Units
Dynamic ODT Timing				
R _{TT} dynamic change skew	t _{ADC}	0.3	0.7	t _{CK} (AVG)
Write Leveling Timing				
First DQS, /DQS rising edge	t _{WLMRD}	40	-	t _{CK}
DQS, /DQS delay	t _{WLDQSEN}	25	-	t _{CK}
Write leveling setup from rising CK, /CK crossing to rising DQS, /DQS crossing	t _{WLS}	165	-	ps
Write leveling hold from rising DQS, /DQS crossing to rising CK, /CK crossing	t _{WLH}	165	-	ps
Write leveling output delay	t _{WLO}	0	7.5	ns
Write leveling output error	t _{WLOE}	0	2	ns

For part number IMM2G64D3(L)SOD8AG-B125(I)

Table 19 - SPD Information

Byte NO.	Description	Note		Hex	
		1.35V Operation	1.5V Operation	1.35V Operation	1.5V Operation
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	176 / 256 / 0-116		92	
1	SPD Revision	1.2		12	
2	Key Byte / DRAM Device Type	DDR3 SDRAM		0B	
3	Key Byte / Module Type	64b Unbuffered SO-DIMM		03	
4	SDRAM Density and Banks	8Gb 8banks		05	
5	SDRAM Addressing	Row 16 / Col 11		22	
6	Module Nominal Voltage, VDD	1.35V/1.5V	1.5V	02	00
7	Module Organization	2Rank , x8		09	
8	Module Memory Bus Width	Non-ECC, 64bit		03	
9	Fine Timebase (FTB) Dividend and Divisor	2.5ps		52	
10	Medium Timebase (MTB) Dividend	1/8 (0.125ns)		01	
11	Medium Timebase (MTB) Divisor	1/8 (0.125ns)		08	
12	SDRAM Minimum Cycle Time (tCKmin)	1.25ns		0A	
13	Reserved	-		00	
14	CAS Latencies Supported, Least Significant Byte	5, 6, 7, 8, 9, 10, 11		FE	
15	CAS Latencies Supported, Most Significant Byte	-		00	
16	Minimum CAS Latency Time (tAamin)	13.125ns		69	
17	Minimum Write Recovery Time (tWRmin)	15ns		78	
18	Minimum /RAS to /CAS Delay Time (tRCDmin)	13.125ns		69	
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	7.5ns		3C	
20	Minimum Row Precharge Time (tRPmin)	13.125ns		69	
21	Upper Nibbles for tRAS and tRC	-		11	
22	Minimum Active to Precharge Time (tRASmin), LSB	35ns		18	
23	Minimum Active to Active/Refresh Time (tRCmin), LSB	48.125ns		81	
24	Minimum Refresh Recovery Time (tRFCmin), LSB	300ns		60	
25	Minimum Refresh Recovery Time (tRFCmin), MSB	300ns		09	
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	7.5ns		3C	
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns		3C	
28	Upper Nibble for tFAW	40ns		01	
29	Minimum Four Activate Window Delay Time (tFAWmin), LSB	40ns		40	
30	SDRAM Optional Features	DLL off Mode, RZQ/6, RZQ/7		83	
31	SDRAM Thermal and Refresh Options	0-95oC Op. Temp. w/2x refresh		05	
32	Module Thermal Sensor	Without TS		00	
33	SDRAM Device Type	Non-Standard SDRAM		A1	
34-59	Reserved, General Section	-		00	
60	Module Nominal Height	29< Height <= 30		0F	

Byte NO.	Description	Note	Hex
61	Module Maximum Thickness	1 < Tf ≤ 2 (mm); 1 < Tb ≤ 2 (mm)	11
62	Reference Raw Card Used	Raw Card F3	65
63	Address Mapping from Edge Connector to DRAM	Non-Mirrored	00
64-116	Module Type Specific Section, Indexed by Key Byte	-	00
117-118	Module ID: Module Manufacturer's JEDEC ID Code	Reserved	Reserved
119	Module ID: Module Manufacturing Location	Reserved	Reserved
120-121	Module ID: Module Manufacturing Date	Reserved	Reserved
122-125	Module ID: Module Serial Number	Reserved	Reserved
126-127	Cyclical Redundancy Code	-	2A 50 81 D7
128-145	Module Part Number	Reserved	Reserved
146-147	Module Revision Code	Reserved	Reserved
148-149	DRAM Manufacturer's JEDEC ID Code	Reserved	Reserved
150-175	Manufacturer's Specific Data	Reserved	Reserved
176-255	Open For Customer Use	Reserved	Reserved

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