

Datasheet | Rev. 3.0 | 2015

IMM2G72D3(L)RVD8AG (Die Revision B) 16GByte (2048M x 72 Bit)

16GB DDR3 VLP Registered DIMM
RoHS Compliant Product

Version: Rev. 3.0, JUN 2015

- 3.0 – Updated tRFC in Table 18
- Revised SPD Information in Table 19

Version: Rev. 2.0, JUL 2014

- 2.0 – Updated CAS Latency support to include CL5
- Added Operation temperature for Industrial Temperature Product in Table 10
- Updated Input Switching Conditions in Table 13
- Moved V_{SEH} information from Table 14 to Table 15
- Updated IDD values in Table 17
- Updated tAA, tRCD, tRRD, tRP, tFAW in Table 18, 19

Version: Rev. 1.0, NOV 2013

- 1.0 - Initial release

Remark:

Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures .

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Features

- 240-Pin Registered Dual-In-Line Memory Module
- Capacity: 16GB
- JEDEC-Standard
- Bi-directional Differential Data-Strobe
- 72 Bit Data Bus Width with ECC
- Programmable CAS Latency (CL):
 - PC3-12800: 5, 6, 7, 8, 9, 10, 11
 - PC3-10600: 5, 6, 7, 8, 9
- Programmable CAS Write Latency (CWL):
 - PC3-12800: 5, 6, 7, 8
 - PC3-10600: 5, 6, 7
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- On-Die Termination (ODT)
- ZQ Calibration Supported
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Asynchronous Reset
- On-board I2C Temperature Sensor with Integrated Serial Presence Detect (SPD) EEPROM
- Gold Edge Contacts
- 100% RoHS-Compliant
- Very Low Profile Module Height: 18.75mm (0.738 inch)

Table 1 - Ordering Information for RoHS Compliant Product

Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM2G72D3xRVD8AG-Bzzzy	16GB	2Gx72	2	16GB DDR3 VLP Registered DIMM

Notes:

- x: Operating Voltage
- y: Operating Temperature
- zzz: Speed Grade

Table 2 - Operating Voltage

Part Number	Operating Voltage
Blank	VDD, VDDQ = 1.5V (1.425V-1.575V)
L	VDD, VDDQ = 1.35V (1.283V-1.45V) Backward compatible to VDD, VDDQ = 1.5V (1.425V-1.575V)

Table 3 - Temperature Grade

Part Number	Temperature Grade	T _{case}
Blank	Commercial temperature	0°C to 95°C
I	Industrial temperature	-40°C to 95°C

Remark: T_{case} is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85°C < T_{case} <= 95°C.

Table 4 - Speed Grade

Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
125	PC3-12800 (DDR3-1600)	800MHz (1.25ns@CL=11)
15E	PC3-10600 (DDR3-1333)	667MHz (1.5ns@CL=9)

Table 5 - Memory Chip Information

Part Number	Base Device Brand	Base device	Voltage	Type	Chip Packing
IMM2G72D3LRVD8AG-Bzzzy	I'M	IM8G08D3FBGG	1.35V	1024Mx8	Lead Free
IMM2G72D3RVD8AG-Bzzzy	I'M	IM8G08D3EBGG	1.5V	1024Mx8	Lead Free

Part Number Decoder

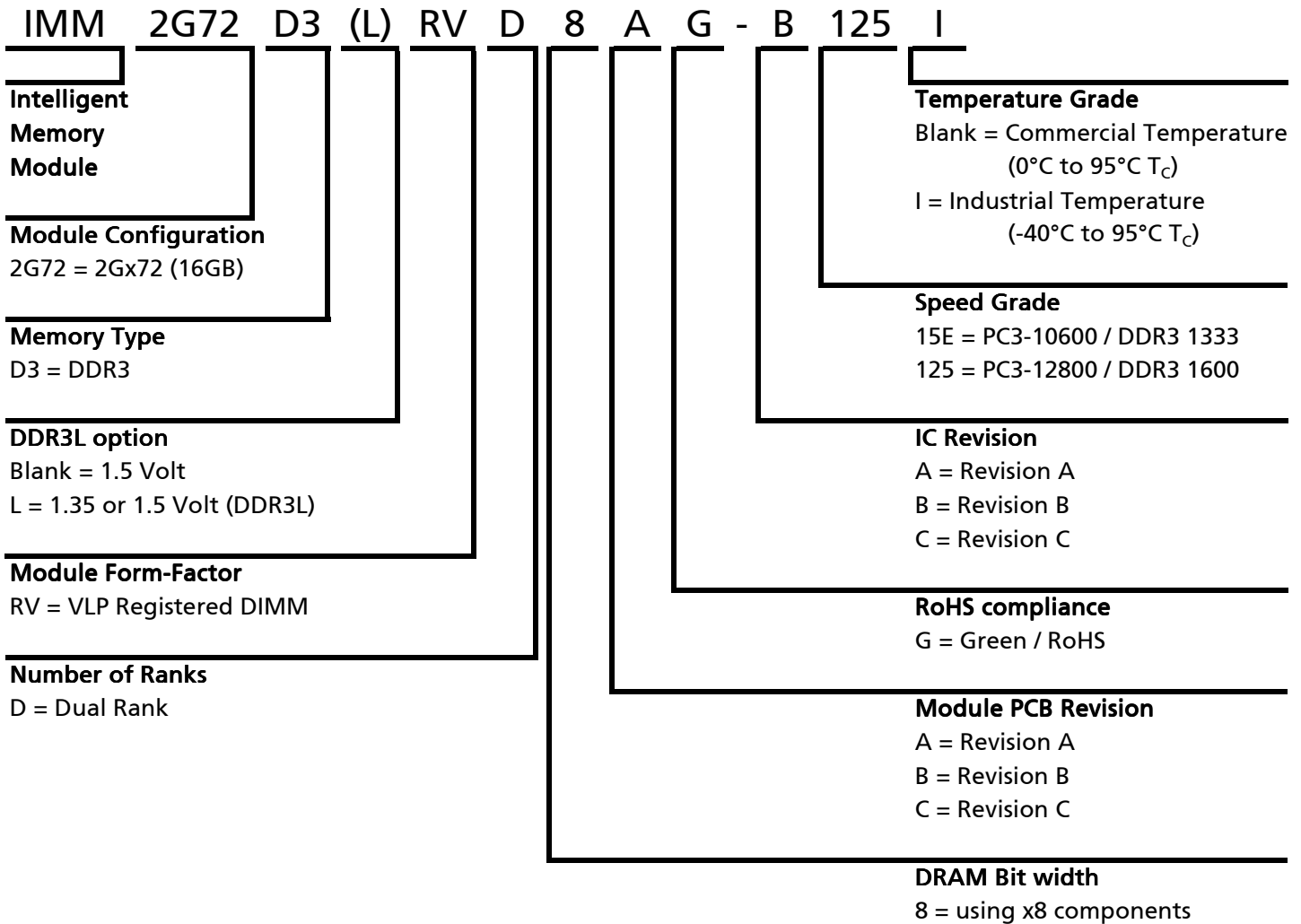


Table 6 - Addressing

Parameter	16GB
Refresh count	8K
Row address	64K A[15:0]
Device bank address	8 BA[2:0]
Device configuration	8Gb (1024Mx8)
Column address	2K A[9:0], A11
Module rank address	2 /S[1:0]
Number of devices	18

Table 7 – Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	121	VSS	61	A2	181	A1
2	VSS	122	DQ4	62	VDD	182	VDD
3	DQ0	123	DQ5	63	CK1	183	VDD
4	DQ1	124	VSS	64	/CK1	184	CK0
5	VSS	125	DM0,TDQS9	65	VDD	185	/CK0
6	/DQS0	126	NC,/TDQS9	66	VDD	186	VDD
7	DQS0	127	VSS	67	VREFCA	187	/EVENT
8	VSS	128	DQ6	68	Par_In	188	A0
9	DQ2	129	DQ7	69	VDD	189	VDD
10	DQ3	130	VSS	70	A10/AP	190	BA1
11	VSS	131	DQ12	71	BA0	191	VDD
12	DQ8	132	DQ13	72	VDD	192	/RAS
13	DQ9	133	VSS	73	/WE	193	/S0
14	VSS	134	DM1,TDQS10	74	/CAS	194	VDD
15	/DQS1	135	NC,/TDQS10	75	VDD	195	ODT0
16	DQS1	136	VSS	76	/S1	196	A13
17	VSS	137	DQ14	77	ODT1	197	VDD
18	DQ10	138	DQ15	78	VDD	198	NC
19	DQ11	139	VSS	79	NC	199	VSS
20	VSS	140	DQ20	80	VSS	200	DQ36
21	DQ16	141	DQ21	81	DQ32	201	DQ37
22	DQ17	142	VSS	82	DQ33	202	VSS
23	VSS	143	DM2,TDQS11	83	VSS	203	DM4,TDQS13
24	/DQS2	144	NC,/TDQS11	84	/DQS4	204	NC,/TDQS13
25	DQS2	145	VSS	85	DQS4	205	VSS
26	VSS	146	DQ22	86	VSS	206	DQ38
27	DQ18	147	DQ23	87	DQ34	207	DQ39
28	DQ19	148	VSS	88	DQ35	208	VSS
29	VSS	149	DQ28	89	VSS	209	DQ44
30	DQ24	150	DQ29	90	DQ40	210	DQ45
31	DQ25	151	VSS	91	DQ41	211	VSS
32	VSS	152	DM3,TDQS12	92	VSS	212	DM5,TDQS14
33	/DQS3	153	NC,/TDQS12	93	/DQS5	213	NC,/TDQS14
34	DQS3	154	VSS	94	DQS5	214	VSS
35	VSS	155	DQ30	95	VSS	215	DQ46
36	DQ26	156	DQ31	96	DQ42	216	DQ47
37	DQ27	157	VSS	97	DQ43	217	VSS
38	VSS	158	CB4	98	VSS	218	DQ52
39	CB0	159	CB5	99	DQ48	219	DQ53
40	CB1	160	VSS	100	DQ49	220	VSS
41	VSS	161	DM8,TDQS17	101	VSS	221	DM6,TDQS15
42	/DQS8	162	NC,/TDQS17	102	/DQS6	222	NC,/TDQS15
43	DQS8	163	VSS	103	DQS6	223	VSS
44	VSS	164	CB6	104	VSS	224	DQ54
45	CB2	165	CB7	105	DQ50	225	DQ55
46	CB3	166	VSS	106	DQ51	226	VSS
47	VSS	167	NC	107	VSS	227	DQ60
48	VTT	168	/RESET	108	DQ56	228	DQ61
49	VTT	169	CKE1	109	DQ57	229	VSS
50	CKE0	170	VDD	110	VSS	230	DM7,TDQS16
51	VDD	171	A15	111	/DQS7	231	NC,/TDQS16
52	BA2	172	A14	112	DQS7	232	VSS
53	/Err_Out	173	VDD	113	VSS	233	DQ62
54	VDD	174	A12, /BC	114	DQ58	234	DQ63
55	A11	175	A9	115	DQ59	235	VSS
56	A7	176	VDD	116	VSS	236	VDDSPD
57	VDD	177	A8	117	SA0	237	SA1
58	A5	178	A6	118	SCL	238	SDA

Pin	Name	Pin	Name	Pin	Name	Pin	Name
59	A4	179	VDD	119	SA2	239	VSS
60	VDD	180	A3	120	VTT	240	VTT

Table 8 - Pin Description

Pin Name	Description	Pin Name	Description
VDD	SDRAM core power supply	VREFDQ	SDRAM I/O reference supply
VREFCA	SDRAM command/address reference supply	VSS	Power supply return (ground)
A0-A15	SDRAM address bus	BA0-BA2	SDRAM bank addresses
CK0-CK1	SDRAM clocks (positive line of differential pair)	/CK0-/CK1	SDRAM clocks (negative line of differential pair)
/RAS	SDRAM row address strobe	/CAS	SDRAM column address strobe
/WE	SDRAM write enable	CKE0-CKE1	SDRAM clock enable lines
/S0-/S1	DIMM Rank Select Lines	ODT0-ODT1	On-die termination control lines
DQS0-DQS8	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS8	SDRAM data strobes (negative line of differential pair)
TDQS9-TDQ17	Termination data strobes (positive line of differential pair)	/TDQS9-/TDQS17	Termination data strobes (negative line of differential pair)
D0-D63	DIMM memory data bus	DM0-DM8	SDRAM data mask/high data strobes
CB0-CB7	DIMM ECC Check bit	Par_In	Parity bit for the Address and Control bus
/Err_Out	Parity error detected on the Address and Control bus	/EVENT	Temperature event
SCL	EEPROM clock	SDA	EEPROM data line
SA0-SA1	EEPROM address input	VDDSPD	EEPROM positive power supply
/RESET	Reset Pin	VTT	Termination Voltage
NC	Spare Pins (no connect)		

Figure 1 – Module Dimension 240 Pin DDR3 SDRAM VLP Registered DIMM

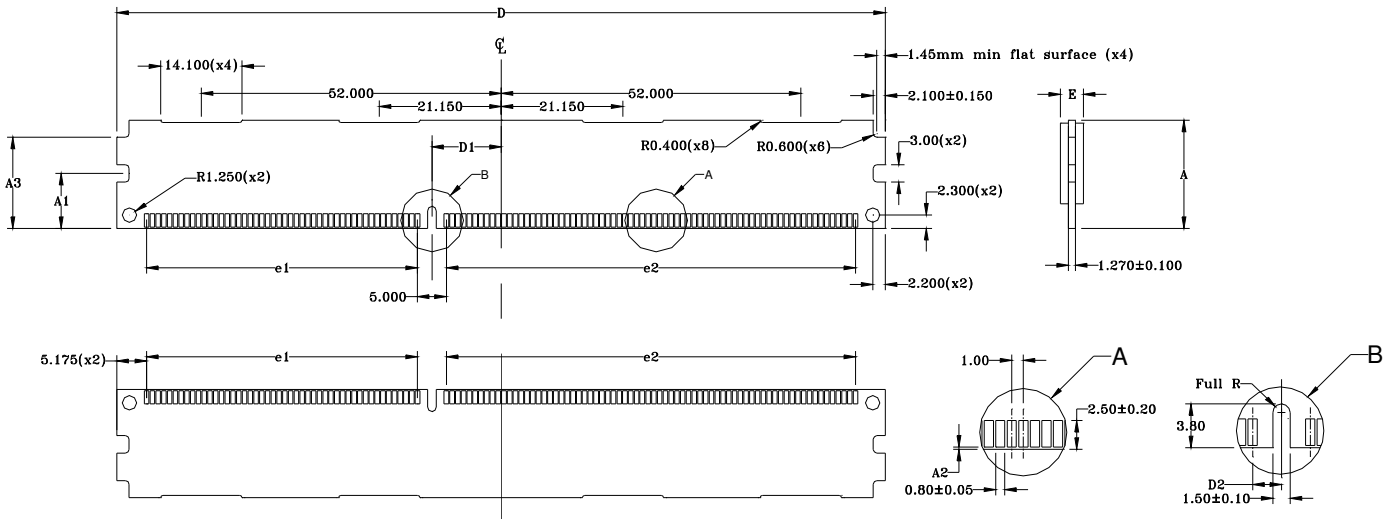


Table 9 - PCB Dimension

Symbol	MIN	NOM	MAX
A	18.60	18.75	18.90
A1	9.35	9.50	9.65
A2	0.05	0.20	0.36
A3	15.65	15.80	15.95
D	133.20	133.35	133.50
D1	12.00 Basic		
D2	2.50 Basic		
e1	47.00 Basic		
e2	71.00 Basic		
E			4.00

Notes:

- All dimensioning and tolerancing conform to ASME Y14.5M-1994.
- Tolerances for all dimensions ± 0.15 unless otherwise specified.
- All dimensions are in millimeters.

Figure 2 – Functional Block Diagram (Page 1 of 4)

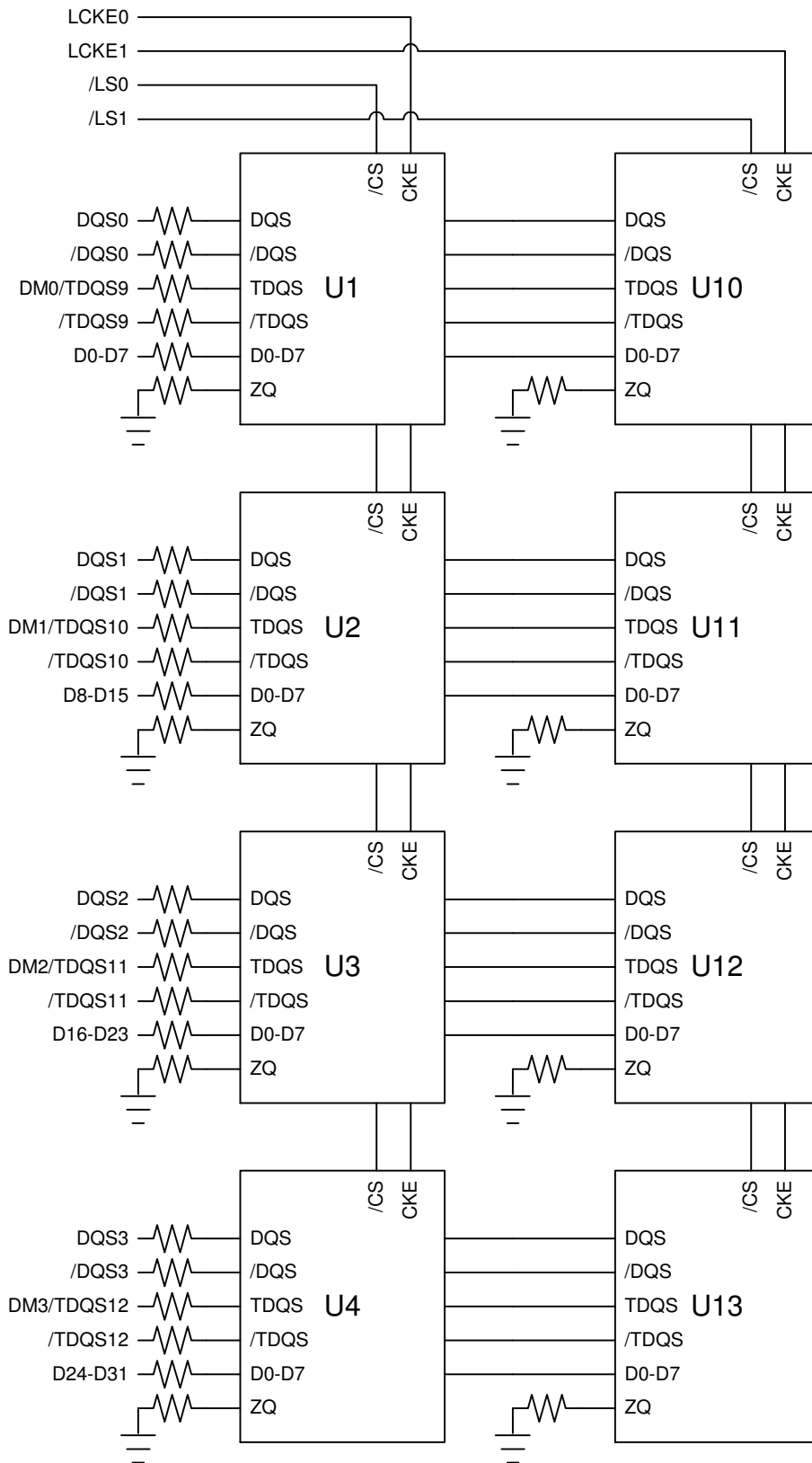


Figure 3 – Functional Block Diagram (Page 2 of 4)

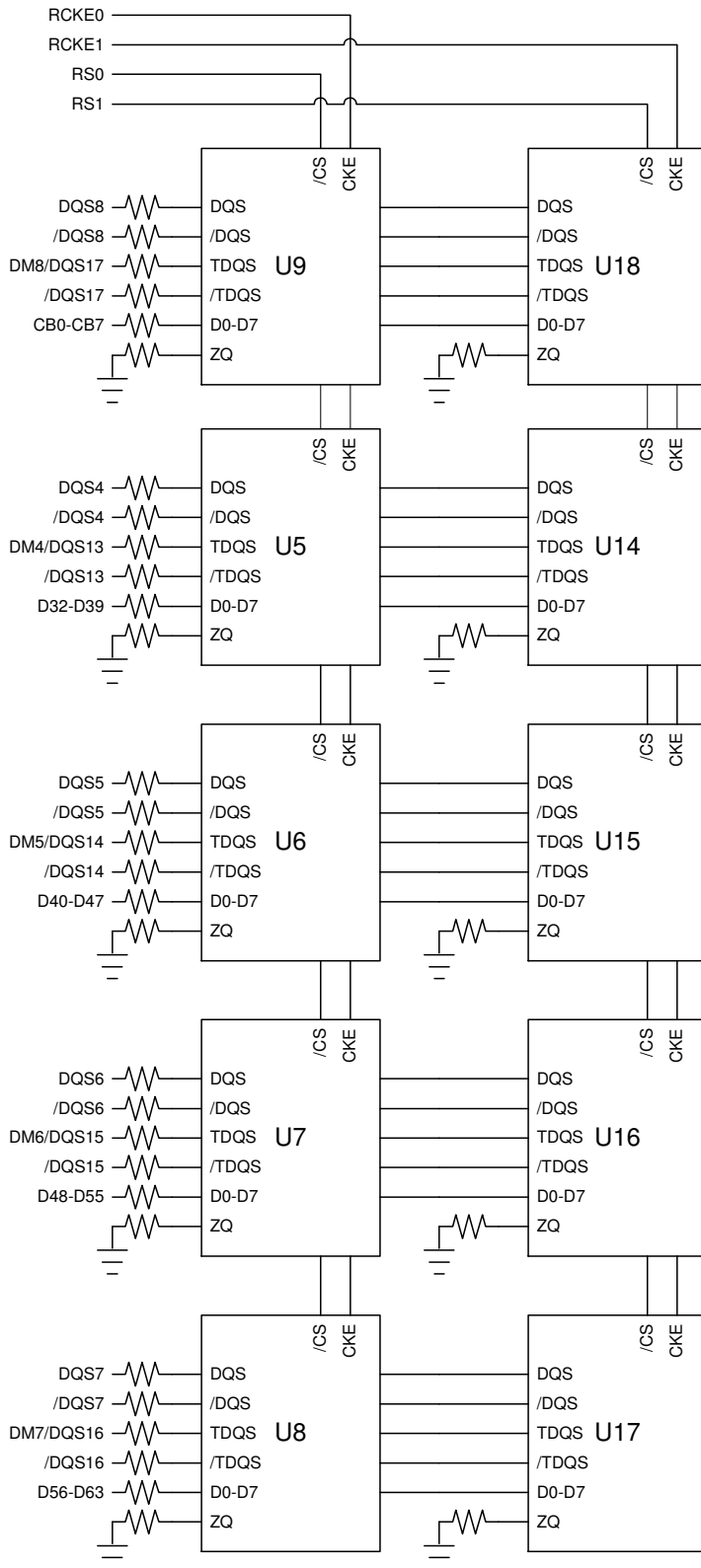


Figure 4 – Functional Block Diagram (Page 3 of 4)

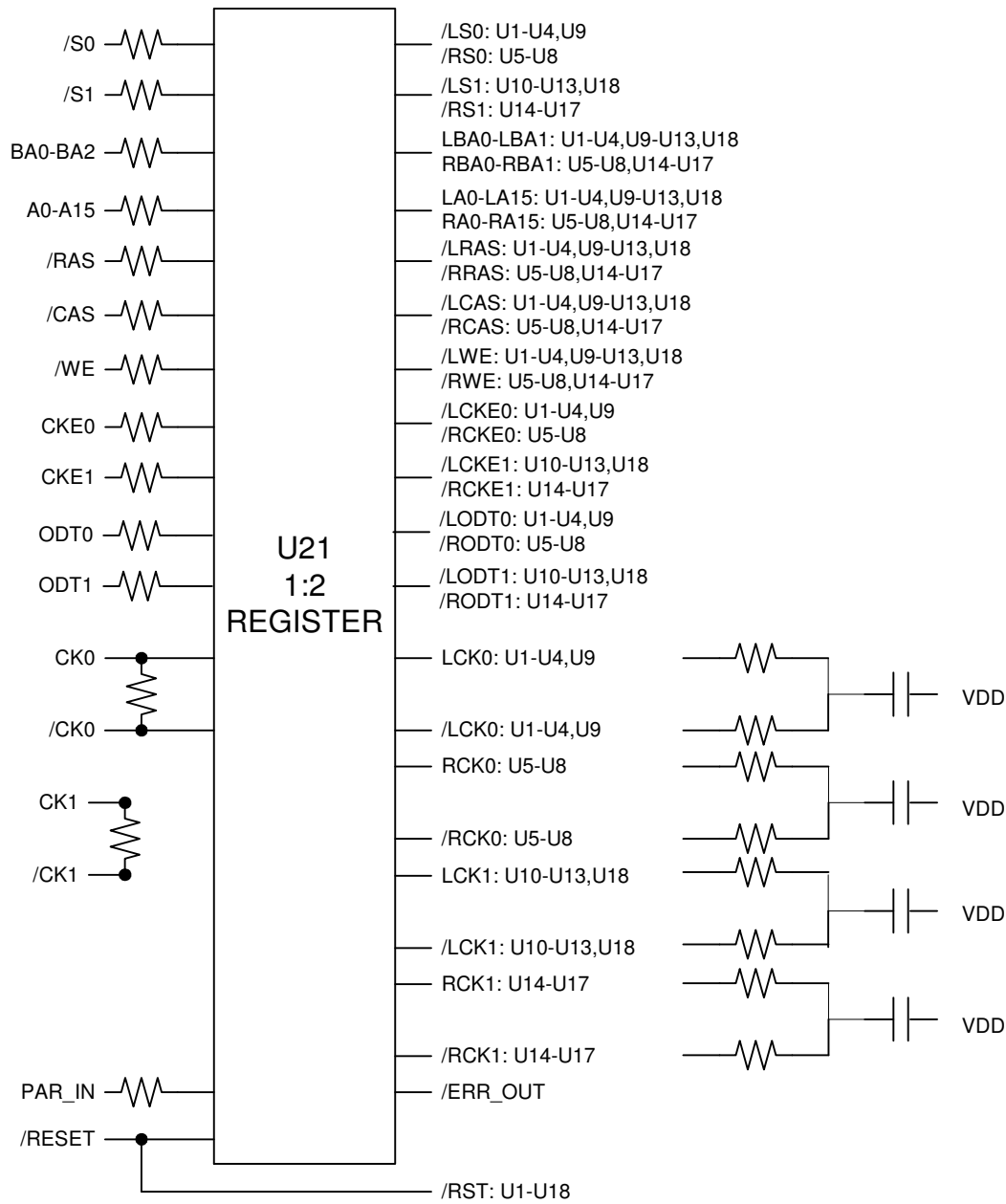
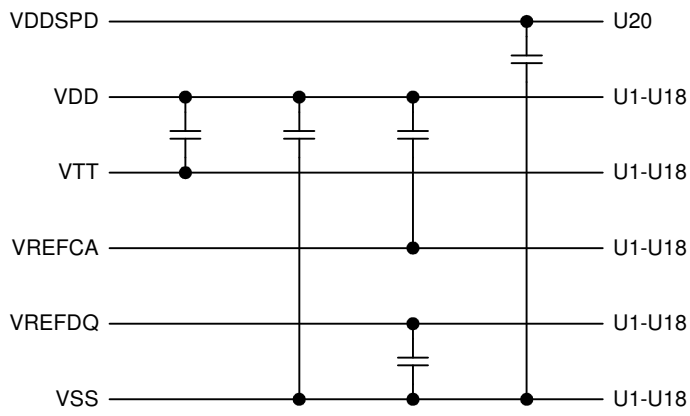
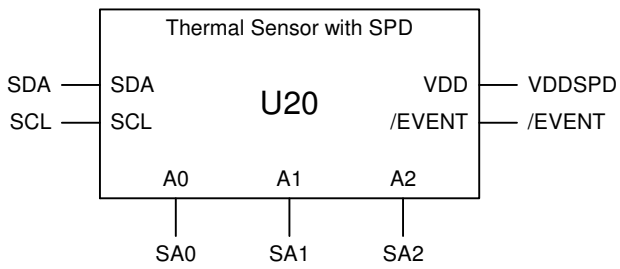


Figure 5 – Functional Block Diagram (Page 4 of 4)



All address / command / control VTT



Electrical Parameter

Table 10 - Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on V _{DD} , pin relative to V _{SS}	V _{DD}	-0.4V ~ 1.975	V	1,3
Voltage on V _{DDQ} , pin relative to V _{SS}	V _{DDQ}	-0.4V ~ 1.975	V	1,3
Voltage on any pins relative to V _{SS}	V _{IN} , V _{OUT}	-0.4V ~ 1.975	V	1
DRAM Storage temperature	T _{STG}	-55 ~ 100	°C	1,2
DRAM Operation temperature (Standard Product)	T _{case}	0 ~ 95	°C	2,4,6
DRAM Operation temperature (Industrial Temperature Product)	T _{case}	-40 ~ 95	°C	2,5,6

Notes:

- ¹ Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- ² Storage Temperature or DRAM operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC51-2 standard.
- ³ VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6 x VDDQ, when VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.
- ⁴ The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-95 °C under all operating conditions.
- ⁵ The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between -40-95 °C under all operating conditions.
- ⁶ Some applications require operation of the Extended Temperature Range between 85 °C and 95 °C case temperature. Full Specifications are guaranteed in this range but the following additional conditions apply
 - a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us.
 - b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

Table 11 - DC Electrical Characteristics and Operating Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ.	Max		
Supply voltage	V _{DD}	1.283	1.35	1.45	V	1,2
I/O supply voltage	V _{DDQ}				V	1,2
Supply voltage	V _{DD}	1.425	1.5	1.575	V	1,2,3
I/O supply voltage	V _{DDQ}				V	1,2,3

Notes:

- ¹ VDD and VDDQ must track one another. VDDQ must be less than or equal to VDD. VSS = VSSQ.
- ² VDD and VDDQ may include AC noise of +/-50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. VDD and VDDQ must be at same level for valid AC timing parameters.
- ³ Module is backward-compatible with 1.5V operation.

Table 12 - DC Electrical Characteristics and Input Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ.	Max		
V_{IN} low; DC/commands/address buses (1.35V Operation)	V_{IL}	V_{SS}	-	-0.090	V	
V_{IN} low; DC/commands/address buses (1.5V Operation)	V_{IL}	V_{SS}	-	-0.100	V	
V_{IN} high; DC/commands/address buses (1.35V Operation)	V_{IH}	0.090	-	V_{DD}	V	
V_{IN} high; DC/commands/address buses (1.5V Operation)	V_{IH}	0.100	-	V_{DD}	V	
Input reference voltage; command/address bus	$V_{REFCA(DC)}$	$0.49 * V_{DD}$	$0.50 * V_{DD}$	$0.51 * V_{DD}$	V	1,2
I/O reference voltage DQ bus	$V_{REFDQ(DC)}$	$0.49 * V_{DD}$	$0.50 * V_{DD}$	$0.51 * V_{DD}$	V	2,3
Command/address termination voltage (system level, not direct DRAM input)	V_{TT}	-	$0.50 * V_{DDQ}$	-	V	4

Notes:

- ¹ $V_{REFCA(DC)}$ is expected to be approximately $0.5 \times V_{DD}$ and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFCA} may not exceed $\pm 1\% \times V_{DD}$ around the $V_{REFCA(DC)}$ value. Peak-to-peak AC noise on V_{REFCA} should not exceed $\pm 2\%$ of $V_{REFCA(DC)}$.
- ² DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20 MHz in frequency.
- ³ $V_{REFDQ(DC)}$ is expected to be approximately $0.5 \times V_{DD}$ and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFDQ} may not exceed $\pm 1\% \times V_{DD}$ around the $V_{REFDQ(DC)}$ value. Peak-to-peak AC noise on V_{REFDQ} should not exceed $\pm 2\%$ of $V_{REFDQ(DC)}$.
- ⁴ V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors. MIN and MAX values are system-dependent.

Table 13 - Input Switching Conditions

Parameter / Condition	Symbol	Value		Units
		1.35V Operation	1.5V Operation	
Command and Address				
Input high AC voltage: Logic 1 @ 175mV	$V_{IH(AC175)min}$	-	175	mV
Input high AC voltage: Logic 1 @ 160mV	$V_{IH(AC160)min}$	160	-	mV
Input high AC voltage: Logic 1 @ 150mV	$V_{IH(AC150)min}$	-	150	mV
Input high AC voltage: Logic 1 @ 135mV	$V_{IH(AC135)min}$	135	-	mV
Input high DC voltage: Logic 1 @ 100mV	$V_{IH(DC100)min}$	-	100	mV
Input high DC voltage: Logic 1 @ 90mV	$V_{IH(DC90)min}$	90	-	mV
Input low DC voltage: Logic 0 @ -90mV	$V_{IL(DC90)max}$	-90	-	mV
Input low DC voltage: Logic 0 @ -100mV	$V_{IL(DC100)max}$	-	-100	mV
Input low AC voltage: Logic 0 @ -135mV	$V_{IL(AC135)max}$	-135	-	mV
Input low AC voltage: Logic 0 @ -150mV	$V_{IL(AC150)max}$	-	-150	mV
Input low AC voltage: Logic 0 @ -160mV	$V_{IL(AC160)max}$	-160	-	mV
Input low AC voltage: Logic 0 @ -175mV	$V_{IL(AC175)max}$	-	-175	mV

Parameter / Condition	Symbol	Value		Units
		1.35V Operation	1.5V Operation	
DQ and DM				
Input high AC voltage: Logic 1	$V_{IH(AC150)min}$	-	150	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}$	135	-	mV
Input high DC voltage: Logic 1	$V_{IH(DC100)min}$	-	100	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	-	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)max}$	-90	-	mV
Input low DC voltage: Logic 0	$V_{IL(DC100)max}$	-	-100	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)max}$	-135	-	mV
Input low AC voltage: Logic 0	$V_{IL(AC150)max}$	-	-150	mV

Notes:

- 1 All voltages are referenced to VREF. VREF is VREFCA for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. VREF is VREFDQ for DQ and DM inputs.
- 2 Input setup timing parameters (tIS and tDS) are referenced at VIL(AC)/VIH(AC), not VREF(DC).
- 3 Input hold timing parameters (tIH and tDH) are referenced at VIL(DC)/VIH(DC), not VREF(DC).
- 4 Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).

Table 14 - Differential Input Operating Conditions (CK, /CK and DQS, /DQS)

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Differential input voltage logic high – slew (1.35V Operation)	$V_{IH,diff}$	+180	-	mV	1
Differential input voltage logic high – slew (1.5V Operation)	$V_{IH,diff}$	+200	-	mV	1
Differential input voltage logic low – slew (1.35V Operation)	$V_{IL,diff}$	-	-180	mV	1
Differential input voltage logic low – slew (1.5V Operation)	$V_{IL,diff}$	-	-200	mV	1
Differential input voltage logic high	$V_{IH,diff(AC)}$	$2 * (V_{IH(AC)} - V_{REF})$	-	mV	2
Differential input voltage logic low	$V_{IL,diff(AC)}$	-	$2 * (V_{IL(AC)} - V_{REF})$	mV	3
Differential Input Cross Point Voltage relative to VDD/2 for CK, /CK	V_{IX}	-150	150	mV	
Differential Input Cross Point Voltage relative to VDD/2 for DQS, /DQS	V_{IX}	-150	150	mV	

Notes:

- ¹ Defines slew rate reference points, relative to input crossing voltages.
- ² Minimum DC limit is relative to single-ended signals; overshoot specifications are applicable.
- ³ Maximum DC limit is relative to single-ended signals; undershoot specifications are applicable.

Table 15 - Single-Ended Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{REF} - 0.1 * V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.1 * V_{DDQ}$ (1.35V Operation)	SRQse	1.75	5	V/ns	1,2,3
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{REF} - 0.1 * V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.1 * V_{DDQ}$ (1.5V Operation)	SRQse	2.5	5	V/ns	1,2,3
Single-ended high level for strobes	V_{SEH}	$V_{DDQ}/2 + 175$	-	mV	2
Single-ended high level for CK, /CK		$V_{DD}/2 + 175$	-	mV	2
Single-ended low level for strobes	V_{SEL}	-	$V_{DDQ}/2 - 175$	mV	3
Single-ended low level for CK, /CK		-	$V_{DD}/2 - 175$	mV	3
Single-ended DC high-level output voltage	$V_{OH(DC)}$	$0.8 * V_{DDQ}$		V	1
Single-ended DC mid-level output voltage	$V_{OM(DC)}$	$0.5 * V_{DDQ}$		V	1
Single-ended DC low-level output voltage	$V_{OL(DC)}$	$0.2 * V_{DDQ}$		V	1
Single-ended AC high-level output voltage	$V_{OH(AC)}$	$V_{TT} + 0.1 * V_{DDQ}$		V	1,2
Single-ended AC low-level output voltage	$V_{OL(AC)}$	$V_{TT} - 0.1 * V_{DDQ}$		V	1,2
Test load for AC timing and output slew rates	Output to V_{TT} ($V_{DDQ}/2$) via 25Ω resistor				

Notes:

- ¹ RZQ of 240Ω ($\pm 1\%$) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$, $V_{SSQ} = V_{SS}$).
- ² $V_{TT} = V_{DDQ}/2$.
- ³ The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or all switching the opposite direction. For all other DQ signal switching combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.

Table 16 - Differential Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)} = -0.2 * V_{DDQ}$ and $V_{OH,diff(AC)} = +0.2 * V_{DDQ}$ (1.35V Operation)	SRQ_{diff}	3.5	12	V/ns	1
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)} = -0.2 * V_{DDQ}$ and $V_{OH,diff(AC)} = +0.2 * V_{DDQ}$ (1.5V Operation)	SRQ_{diff}	5	10	V/ns	1
Differential high-level output voltage	$V_{OH,diff(AC)}$	$+0.2 * V_{DDQ}$		V	1
Differential low-level output voltage	$V_{OL,diff(AC)}$	$-0.2 * V_{DDQ}$		V	1
Test load for AC timing and output slew rates	Output to V_{TT} ($V_{DDQ}/2$) via 25Ω resistor				

Notes:

- ¹ RZQ of 240Ω ($\pm 1\%$) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$, $V_{SSQ} = V_{SS}$).
- ² $V_{REF} = V_{DDQ}/2$; slew rate @ 5V/ns, interpolate for faster slew rate.

For part number IMM2G72D3(L)RVD8AG-B125(I)

Table 17 - IDD Specifications with Conditions and Operation Current

Parameter / Condition	Symbol	Current		Units	Notes
		1.35V Operation	1.5V Operation		
Operating current 0; One bank ACTIVATE-to-PRECHARGE	I_{DD0}	1134	1215	mA	1, 2
Operating current 1; One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	1422	1530	mA	1, 2
Precharge power-down current; Slow exit	I_{DD2P0}	504	540	mA	1, 3
Precharge power-down current; Fast exit	I_{DD2P1}	504	540	mA	1, 3
Precharge quiet standby current	I_{DD2Q}	648	720	mA	1, 3
Precharge standby current	I_{DD2N}	1008	1080	mA	1, 3
Precharge standby ODT current	I_{DD2NT}	1188	1260	mA	1, 3
Active power-down current	I_{DD3P}	540	576	mA	1, 3
Active standby current	I_{DD3N}	1116	1260	mA	1, 3
Burst read operating current	I_{DD4R}	2727	2880	mA	1, 2
Burst write operating current	I_{DD4W}	1512	1620	mA	1, 2
Refresh current	I_{DD5B}	2997	3150	mA	1, 2
Self refresh temperature current: MAX $T_c = 85^\circ\text{C}$	I_{DD6}	360	396	mA	1, 3
Self refresh temperature current (SRT-enabled): MAX $T_c = 95^\circ\text{C}$	I_{DD6ET}	360	396	mA	1, 3
All banks interleaved read current	I_{DD7}	3897	4095	mA	1, 2
Reset current	I_{DD8}	414	450	mA	1, 2

Notes:

- ¹ Value shown for DDR3 SDRAM only and are computed from values specified in the 8Gbit component data sheet.
- ² One module rank in the active IDD, the other rank in IDD2P0.
- ³ All ranks in this IDD conditions.

For part number IMM2G72D3(L)RVD8AG-B125(I)

Table 18 - AC Timing Parameter and Operating Conditions						
Parameter / Condition		Symbol	Min	Max	Units	
Clock Timing						
Clock period average: DLL disable mode	$T_c = 0^\circ\text{C to } 85^\circ\text{C}$	$t_{CK}(\text{DLL_DIS})$	8	7800	ns	
	$T_c \Rightarrow 85^\circ\text{C to } 95^\circ\text{C}$		8	3900		
Clock periods average: DLL enable mode (CL = 11, CWL = 8)		$t_{CK}(\text{AVG})$	1.25	<1.5	ns	
Clock periods average: DLL enable mode (CL = 9, CWL = 7)		$t_{CK}(\text{AVG})$	1.5	<1.875	ns	
High pulse width average		$t_{CH}(\text{AVG})$	0.47	0.53	t_{CK}	
Low pulse width average		$t_{CL}(\text{AVG})$	0.47	0.53	t_{CK}	
Clock period jitter	DLL locked	t_{JITper}	-70	70	ps	
	DLL locking	$t_{JITper,lck}$	-60	60	ps	
Clock absolute period		$t_{CK}(\text{ABS})$	$t_{CK}(\text{AVG}) \text{ MIN} + t_{JITper}$	$t_{CK}(\text{AVG}) \text{ MAX} + t_{JITper}$	ps	
Clock absolute high pulse width		$t_{CH}(\text{ABS})$	0.43	-	$t_{CK}(\text{AVG})$	
Clock absolute low pulse width		$t_{CL}(\text{ABS})$	0.43	-	$t_{CK}(\text{AVG})$	
Cycle-to-cycle jitter	DLL locked	t_{JITcc}		140	ps	
	DLL locking	$t_{JITcc,lck}$		120	ps	
Cumulative error across	2 cycles	$t_{ERR2per}$	-103	103	ps	
	3 cycles	$t_{ERR3per}$	-122	122	ps	
	4 cycles	$t_{ERR4per}$	-136	136	ps	
	5 cycles	$t_{ERR5per}$	-147	147	ps	
	6 cycles	$t_{ERR6per}$	-155	155	ps	
	7 cycles	$t_{ERR7per}$	-163	163	ps	
	8 cycles	$t_{ERR8per}$	-169	169	ps	
	9 cycles	$t_{ERR9per}$	-175	175	ps	
	10 cycles	$t_{ERR10per}$	-180	180	ps	
	11 cycles	$t_{ERR11per}$	-184	184	ps	
	12 cycles	$t_{ERR12per}$	-188	188	ps	
	n = 14,...49, 50 cycles	$t_{ERRnper}$	$(1+0.68\ln[n]) * t_{JITper}$	MIN	$(1+0.68\ln[n]) * t_{JITper}$	Max ps
	DQ Input Timing					
Data setup time to DQS, /DQS (1.35V Operation)	Base (specification)	$t_{DS}(\text{AC135})$	25	-	ps	
					ps	
Data setup time to DQS, /DQS (1.5V Operation)	Base (specification)	$t_{DS}(\text{AC150})$	10	-	ps	
					ps	
Data hold time from DQS, /DQS (1.35V Operation)	Base (specification)	$t_{DH}(\text{DC90})$	55	-	ps	
					ps	
Data hold time from DQS, /DQS (1.5V Operation)	Base (specification)	$t_{DH}(\text{DC100})$	45	-	ps	
					ps	
Minimum data pulse width		t_{DIPW}	360	-	ps	
DQ Output Timing						
DQS, /DQS to DQ skew, per access		t_{DQSQ}	-	100	ps	
DQ output hold time from DQS, /DQS		t_{QH}	0.38	-	$t_{CK}(\text{AVG})$	
DQ Low-Z time from CK, /CK		t_{LZDQ}	-450	225	ps	
DQ High-Z time from CK, /CK		t_{HZDQ}	-	225	ps	
DQ Strobe Input Timing						
DQS, /DQS rising to CK, /CK rising		t_{DQSS}	-0.27	0.27	t_{CK}	
DQS, /DQS differential input low pulse width		t_{DQSL}	0.45	0.55	t_{CK}	

For part number IMM2G72D3(L)RVD8AG-B125(I)

Parameter / Condition		Symbol	Min	Max	Units
DQS, /DQS falling setup to CK, /CK rising		^t DSS	0.18	-	^t CK
DQS, /DQS falling hold from CK, /CK rising		^t DSH	0.18	-	^t CK
DQS, /DQS differential input high pulse width		^t DQSH	0.45	0.55	^t CK
DQS, /DQS differential WRITE preamble		^t WPRE	0.9	-	^t CK
DQS, /DQS differential WRITE postamble		^t WPST	0.3	-	^t CK
DQ Strobe Output Timing					
DQS, /DQS rising to/from CK, /CK		^t DQSK	-225	225	ps
DQS, /DQS differential output high time		^t QSH	0.40	-	^t CK
DQS, /DQS differential output low time		^t QSL	0.40	-	^t CK
DQS, /DQS Low-Z time (RL-1)		^t LZDQS	-450	225	ps
DQS, /DQS High-Z time (RL+BL/2)		^t HZDQS	-	225	ps
DQS, /DQS differential READ preamble		^t RPRE	0.9	greater of ^t LZ(DQS) (MIN), ^t DQSK (MAX)	^t CK
DQS, /DQS differential READ postamble		^t RPST	0.3	greater of ^t DQSK (MIN) + ^t QSH (MIN), ^t HZ(DQS) (MAX)	^t CK
Command and Address Timing					
DLL locking time		^t DLLK	512	-	^t CK
CTRL, CMD, ADDR setup to CK, /CK (1.35V Operation)	Base (specification)	^t IS (AC160)	60	-	ps
					ps
CTRL, CMD, ADDR setup to CK, /CK (1.5V Operation)	Base (specification)	^t IS (AC175)	45	-	ps
CTRL, CMD, ADDR setup to CK, /CK (1.35V Operation)	Base (specification)	^t IS (AC135)	185	-	ps
					ps
					ps
CTRL, CMD, ADDR setup to CK, /CK (1.5V Operation)	Base (specification)	^t IS (AC150)	170	-	ps
					ps
CTRL, CMD, ADDR hold from CK, /CK (1.35V Operation)	Base (specification)	^t IH (DC90)	130	-	ps
					ps
CTRL, CMD, ADDR hold from CK, /CK (1.5V Operation)	Base (specification)	^t IH (DC100)	120	-	ps
					ps
Minimum CTRL, CMD, ADDR pulse width		^t IPW	560	-	ps
ACTIVATE to internal READ or WRITE delay		^t RCD	13.125	-	ns
PRECHARGE command period		^t RP	13.125	-	ns
ACTIVATE-to-PRECHARGE command period		^t RAS	35	9 * ^t REFI	ns
ACTIVATE-to-ACTIVATE command period		^t RC	48.125	-	ns
ACTIVATE-to-ACTIVATE minimum period		^t RRD	greater of 4 ^t CK or 7.5ns	-	^t CK
Four ACTIVATE windows (2KB page size)		^t FAW	40	-	ns
Write recovery time		^t WR	15	-	ns
Delay from start of internal WRITE transaction to internal READ command		^t WTR	greater of 4 ^t CK or 7.5ns	-	^t CK
READ-to-PRECHARGE time		^t RTP	greater of 4 ^t CK or 7.5ns	-	^t CK
/CAS-to-/CAS command delay		^t CCD	4	-	^t CK
Auto precharge write recovery + precharge time		^t DAL	WR + ^t RP/ ^t CK (AVG)	-	^t CK
MODE REGISTER SET command cycle time		^t MRD	4	-	^t CK
MODE REGISTER SET command update delay		^t MOD	greater of 12 ^t CK or 15ns	-	^t CK
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		^t MPPRR	1	-	^t CK

For part number IMM2G72D3(L)RVD8AG-B125(I)

Parameter / Condition		Symbol	Min	Max	Units
Calibration Timing					
ZQCL command: Long calibration time	POWER-UP and RESET operation	t_{ZQinit}	greater of 512 t_{CK}	-	t_{CK}
	Normal operation	t_{ZQoper}	greater of 256 t_{CK}	-	t_{CK}
ZQCS command: Short calibration time		t_{ZQcs}	greater of 64 t_{CK}	-	t_{CK}
Initialization and Reset Timing					
Exit reset from CKE HIGH to valid command		t_{XPR}	greater of 5 t_{CK} or $t_{RFC(min)}+10ns$	-	t_{CK}
Refresh Timing					
REFRESH-to-ACTIVATE or REFRESH command period		t_{RFC}	300	-	ns
Maximum refresh period	$T_{c} \leq 85^{\circ}C$	-	64 (1X)	-	ms
	$T_{c} > 85^{\circ}C$	-	32 (2X)	-	ms
Maximum average periodic refresh	$T_{c} \leq 85^{\circ}C$	t_{REFI}	7.8 (64ms/8192)	-	us
	$T_{c} > 85^{\circ}C$	t_{REFI}	3.9 (32ms/8192)	-	us
Self Refresh Timing					
Exit self refresh to commands not requiring a locked DLL		t_{XS}	greater of 5 t_{CK} or $t_{RFC}+10ns$	-	t_{CK}
Exit self refresh to commands requiring a locked DLL		t_{XSDLL}	$t_{DLLK} (MIN)$	-	t_{CK}
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		t_{CKESR}	$t_{CKE} (MIN) + t_{CK}$	-	t_{CK}
Valid clocks after self refresh entry or power down entry		t_{CKSRE}	greater of 5 t_{CK} or 10ns	-	t_{CK}
Valid clocks before self refresh exit, power-down exit, or reset exit		t_{CKSRX}	greater of 5 t_{CK} or 10ns	-	t_{CK}
Power-Down Timing					
CKE MIN pulse width		$t_{CKE} (MIN)$	greater of 3 t_{CK} or 5ns	-	t_{CK}
Command pass disable delay		t_{CPDED}	1	-	t_{CK}
Power-down entry to power exit timing		t_{PD}	$t_{CKE} (MIN)$	9 * t_{REFI}	t_{CK}
Power-Down Entry Minimum Timing					
ACTIVATE command to power-down entry		$t_{ACTPDEN}$	1	-	t_{CK}
PRECHARGE/PRECHARGE ALL command to power-down entry		t_{PRPDEN}	1	-	t_{CK}
REFRESH command to power-down entry		$t_{REFPDEN}$	1	-	t_{CK}
MRS command to power-down entry		$t_{MRSPDEN}$	MIN = $t_{MOD} (MIN)$	-	t_{CK}
READ/READ with auto precharge command to power-down entry		t_{RDPDEN}	MIN = $RL + 4 + 1$	-	t_{CK}
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	t_{WRPDEN}	MIN = $WL + 4 + t_{WR}/t_{CK} (AVG)$	-	t_{CK}
	BC4MRS	t_{WRPDEN}	MIN = $WL + 2 + t_{WR}/t_{CK} (AVG)$	-	t_{CK}
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	$t_{WRAPDEN}$	MIN = $WL + 4 + t_{WR} + 1$	-	t_{CK}
	BC4MRS	$t_{WRAPDEN}$	MIN = $WL + 2 + t_{WR} + 1$	-	t_{CK}
Power-Down Exit Timing					
DLL on, any valid command, or DLL off to commands not requiring locked DLL		t_{XP}	greater of 3 t_{CK} or 6ns	-	t_{CK}
Precharge power-down with DLL off to commands requiring a locked DLL		t_{XPDLL}	greater of 10 t_{CK} or 24ns	--	t_{CK}

For part number IMM2G72D3(L)RVD8AG-B125(I)

Parameter / Condition	Symbol	Min	Max	Units
ODT Timing				
R _{TT} turn-on from ODTL on reference	t ^{AON}	-225	225	ps
R _{TT} turn-off from ODTL off reference	t ^{AOF}	0.3	0.7	t ^{CK} (AVG)
Asynchronous R _{TT} turn-on delay (power-down with DLL off)	t ^{AONPD}	2	8.5	ns
Asynchronous R _{TT} turn-off delay (power-down with DLL off)	t ^{AOFPD}	2	8.5	ns
ODT high time without write command or with write command and BC4	ODTH4	4	-	t ^{CK}
ODT high time with Write command and BL8	ODTH8	6	-	t ^{CK}
Dynamic ODT Timing				
R _{TT} dynamic change skew	t ^{ADC}	0.3	0.7	t ^{CK} (AVG)
Write Leveling Timing				
First DQS, /DQS rising edge	t ^{WLMRD}	40	-	t ^{CK}
DQS, /DQS delay	t ^{WLDQSEN}	25	-	t ^{CK}
Write leveling setup from rising CK, /CK crossing to rising DQS, /DQS crossing	t ^{WLS}	165	-	ps
Write leveling hold from rising DQS, /DQS crossing to rising CK, /CK crossing	t ^{WLH}	165	-	ps
Write leveling output delay	t ^{WLO}	0	7.5	ns
Write leveling output error	t ^{WLOE}	0	2	ns

For part number IMM2G72D3(L)RVD8AG-B125(I)

Table 19 - SPD Information

Byte NO.	Description	Note		Hex	
		1.35V Operation	1.5V Operation	1.35V Operation	1.5V Operation
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	176 / 256 / 0-116		92	
1	SPD Revision	1.2		12	
2	Key Byte / DRAM Device Type	DDR3 SDRAM		0B	
3	Key Byte / Module Type	Registered DIMM		01	
4	SDRAM Density and Banks	8Gb 8banks		05	
5	SDRAM Addressing	Row 16 / Col 11		22	
6	Module Nominal Voltage, VDD	1.35V/1.5V	1.5V	02	00
7	Module Organization	2Rank , x8		09	
8	Module Memory Bus Width	ECC, 72bit		0B	
9	Fine Timebase (FTB) Dividend and Divisor	2.5ps		52	
10	Medium Timebase (MTB) Dividend	1/8 (0.125ns)		01	
11	Medium Timebase (MTB) Divisor	1/8 (0.125ns)		08	
12	SDRAM Minimum Cycle Time (tCKmin)	1.25ns		0A	
13	Reserved	-		00	
14	CAS Latencies Supported, Least Significant Byte	5, 6, 7, 8, 9, 10, 11		FE	
15	CAS Latencies Supported, Most Significant Byte	-		00	
16	Minimum CAS Latency Time (tAmin)	13.125ns		69	
17	Minimum Write Recovery Time (tWRmin)	15ns		78	
18	Minimum /RAS to /CAS Delay Time (tRCDmin)	13.125ns		69	
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	7.5ns		3C	
20	Minimum Row Precharge Time (tRPmin)	13.125ns		69	
21	Upper Nibbles for tRAS and tRC	-		11	
22	Minimum Active to Precharge Time (tRASmin), LSB	35ns		18	
23	Minimum Active to Active/Refresh Time (tRCmin), LSB	48.125ns		81	
24	Minimum Refresh Recovery Time (tRFCmin), LSB	300ns		60	
25	Minimum Refresh Recovery Time (tRFCmin), MSB	300ns		09	
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	7.5ns		3C	
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns		3C	
28	Upper Nibble for tFAW	40ns		01	
29	Minimum Four Activate Window Delay Time (tFAWmin), LSB	40ns		40	
30	SDRAM Optional Features	DLL off Mode, RZQ/6, RZQ/7		83	
31	SDRAM Thermal and Refresh Options	0-95oC Op. Temp. w/2x refresh		05	
32	Module Thermal Sensor	With TS		80	
33	SDRAM Device Type	Non-Standard SDRAM		A1	
34-59	Reserved, General Section	-		00	
60	Module Nominal Height	18< Height <= 19		04	

Byte NO.	Description	Note		Hex	
		1.35V Operation	1.5V Operation	1.35V Operation	1.5V Operation
61	Module Maximum Thickness	1 < Tf <=2 (mm); 1 < Tb <=2 (mm)		11	
62	Reference Raw Card Used	Raw Card L0		0A	
63	DIMM Module Attributes	2 Rows, 1 Register		09	
64	Heat Spreader Solution	Without HS		00	
65	Register vendor ID code (LSB)	-		00	
66	Register vendor ID code (MSB)	-		00	
67	Register Revision Number	-		FF	
68	Register Type	SSTE32882		00	
69	Register Control Word Function (RC0/RC1)	-		00	
70	Register Control Word Function (RC2/RC3)	Moderate Drive		50	
71	Register Control Word Function (RC4/RC5)	Light Drive		00	
72	Register Control Word Function (RC6/RC7)	-		00	
73	Register Control Word Function (RC8/RC9)	-		00	
74	Register Control Word Function (RC10/RC11)	-		00	
75	Register Control Word Function (RC12/RC13)	-		00	
76	Register Control Word Function (RC14/RC15)	-		00	
77-116	Reserved	-		00	
117-118	Module ID: Module Manufacturer's JEDEC ID Code	Reserved		Reserved	
119	Module ID: Module Manufacturing Location	Reserved		Reserved	
120-121	Module ID: Module Manufacturing Date	Reserved		Reserved	
122-125	Module ID: Module Serial Number	Reserved		Reserved	
126-127	Cyclical Redundancy Code	-		9F 13	34 94
128-145	Module Part Number	Reserved		Reserved	
146-147	Module Revision Code	Reserved		Reserved	
148-149	DRAM Manufacturer's JEDEC ID Code	Reserved		Reserved	
150-175	Manufacturer's Specific Data	Reserved		Reserved	
176-255	Open For Customer Use	Reserved		Reserved	

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