Product Specification | Rev. 1.0 | 2022

IMM512M64D4SOS16AG (Die Revision B)

4GByte (512M x 64 Bit)

4GB DDR4 Unbuffered SO-DIMM
RoHS Compliant Product

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: sales@intelligentmemory.com

Features

- 260-Pin Unbuffered Small Outline Dual-In-Line Memory Module
- Capacity: 4GB
- JEDEC-Standard
- SPD Power Supply: V_{DDSPD} = 2.5 or 3.3V
- Power Supply: V_{DD}, V_{DDQ} = 1.2 ± 0.06V
- DRAM Activating Power Supply: V_{PP} = 2.5V(2.375V – 2.75V)
- Bi-directional Differential Data-Strobe
- 64 Bit Data Bus Width without ECC
- Programmable CAS Latency (CL):
  - DDR4-3200: 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 22, 24
- Programmable CAS Write Latency (CWL):
  - DDR4-3200: 9, 10, 11, 12, 14, 16, 18, 20
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- On-Die Termination (ODT)
- ZQ Calibration Supported
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- Low Power Auto Self Refresh mode is supported
- 8192 Refresh Cycles / 64ms
- Asynchronous Reset
- Serial Presence Detect (SPD) EEPROM
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 30.00mm (1.18inch)

Table 1 - Ordering Information for RoHS Compliant Product				
Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM512M64D4SOS16AG-Bzzzy	4GB	512Mx64	1	4GB DDR4 Unbuffered SO-DIMM

Notes:
y: Operating Temperature
zzz: Speed Grade

Table 2 - Temperature Grade		
Part Number	Temperature Grade	T_{case}^{*}
Blank	Commercial temperature	0°C to 95°C
I	Industrial temperature	-40°C to 95°C

Remark: Tcase is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85 °C < Tcase <= 95 °C.

Table 3 - Speed Grade		
Part Number	Speed Grade	Max. Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
062	DDR4-3200	1600MHz (0.625ns@CL=22)

Table 4 - Memory Chip Information					
Part Number	Base Device Brand	Base device	Voltage	Type	Chip Packing
IMM512M64D4SOS16AG-Bzzzy	IM	IM8G16D4GBBG	1.2V	512Mx16	Lead Free

Part Number Decoder

IM M 512M64 D4 SO S 16 A G - B 062 (I)

IM Module

DRAM Brand
M = IM

Module Configuration
512M64 = 512Mx64 (4GB)

Memory Type
D4 = DDR4

Module Form-Factor
SO = Unbuffered SO-DIMM (SO-UDIMM)

Number of Ranks
S = Single Rank

DRAM Bit width
16 = using x16 components

Module PCB Revision
A = Revision A

RoHS compliance
G = Green / RoHS

IC Revision
B = Revision B

Speed Grade
062 = DDR4-3200 CL22

Temperature Grade
Blank = Commercial Temperature
(0°C to 95°C T_{case})
I = Industrial Temperature
(-40°C to 95°C T_{case})

Table 5 - Addressing

Parameter	4GB
Refresh count	8K
Row address	64K A[15:0]
Device bank address	4 BA[1:0]
Device bank group	2 BG[0]
Device configuration	4Gb (512Mx16)
Column address	1K A[9:0]
Module rank address	1 /S[0]
Number of devices	4

Table 6 – Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	2	V_{SS}	131	A3	132	A2
3	D5	4	D4	133	A1	134	NC
5	V_{SS}	6	V_{SS}	135	V_{DD}	136	V_{DD}
7	D1	8	D0	137	CK0	138	CK1
9	V_{SS}	10	V_{SS}	139	/CK0	140	/CK1
11	/DQS0	12	/DM0, /DBI0	141	V_{DD}	142	V_{DD}
13	DQS0	14	V_{SS}	143	PARITY	144	A0
15	V_{SS}	16	D6	145	BA1	146	A10, AP
17	D7	18	V_{SS}	147	V_{DD}	148	V_{DD}
19	V_{SS}	20	D2	149	/CS0	150	BA0
21	D3	22	V_{SS}	151	A14, /WE	152	/RAS
23	V_{SS}	24	D12	153	V_{DD}	154	V_{DD}
25	D13	26	V_{SS}	155	ODT0	156	A15, /CAS
27	V_{SS}	28	D8	157	NC	158	A13
29	D9	30	V_{SS}	159	V_{DD}	160	V_{DD}
31	V_{SS}	32	/DQS1	161	NC	162	NC
33	/DM1, /DBI1	34	DQS1	163	V_{DD}	164	V_{REFCA}
35	V_{SS}	36	V_{SS}	165	NC	166	SA2
37	D15	38	D14	167	V_{SS}	168	V_{SS}
39	V_{SS}	40	V_{SS}	169	D37	170	D36
41	D10	42	D11	171	V_{SS}	172	V_{SS}
43	V_{SS}	44	V_{SS}	173	D33	174	D32
45	D21	46	D20	175	V_{SS}	176	V_{SS}
47	V_{SS}	48	V_{SS}	177	/DQS4	178	/DM4, /DBI4
49	D17	50	D16	179	DQS4	180	V_{SS}
51	V_{SS}	52	V_{SS}	181	V_{SS}	182	D39
53	/DQS2	54	/DM2, /DBI2	183	D38	184	V_{SS}
55	DQS2	56	V_{SS}	185	V_{SS}	186	D35
57	V_{SS}	58	D22	187	D34	188	V_{SS}
59	D23	60	V_{SS}	189	V_{SS}	190	D45
61	V_{SS}	62	D18	191	D44	192	V_{SS}
63	D19	64	V_{SS}	193	V_{SS}	194	D41
65	V_{SS}	66	D28	195	D40	196	V_{SS}
67	D29	68	V_{SS}	197	V_{SS}	198	/DQS5
69	V_{SS}	70	D24	199	/DM5, /DBI5	200	DQS5
71	D25	72	V_{SS}	201	V_{SS}	202	V_{SS}
73	V_{SS}	74	/DQS3	203	D46	204	D47
75	/DM3, /DBI3	76	DQS3	205	V_{SS}	206	V_{SS}
77	V_{SS}	78	V_{SS}	207	D42	208	D43
79	D30	80	D31	209	V_{SS}	210	V_{SS}
81	V_{SS}	82	V_{SS}	211	D52	212	D53
83	D26	84	D27	213	V_{SS}	214	V_{SS}
85	V_{SS}	86	V_{SS}	215	D49	216	D48
87	NC	88	NC	217	V_{SS}	218	V_{SS}
89	V_{SS}	90	V_{SS}	219	/DQS6	220	/DM6, /DBI6
91	NC	92	NC	221	DQS6	222	V_{SS}
93	V_{SS}	94	V_{SS}	223	V_{SS}	224	D54
95	NC	96	NC	225	D55	226	V_{SS}
97	NC	98	V_{SS}	227	V_{SS}	228	D50
99	V_{SS}	100	NC	229	D51	230	V_{SS}
101	NC	102	V_{SS}	231	V_{SS}	232	D60
103	V_{SS}	104	NC	233	D61	234	V_{SS}
105	NC	106	V_{SS}	235	V_{SS}	236	D57
107	V_{SS}	108	/RESET	237	D56	238	V_{SS}
109	CKE0	110	NC	239	V_{SS}	240	/DQS7
111	V_{DD}	112	V_{DD}	241	/DM7, /DBI7	242	DQS7
113	NC	114	/ACT	243	V_{SS}	244	V_{SS}
115	BG0	116	/ALERT	245	D62	246	D63

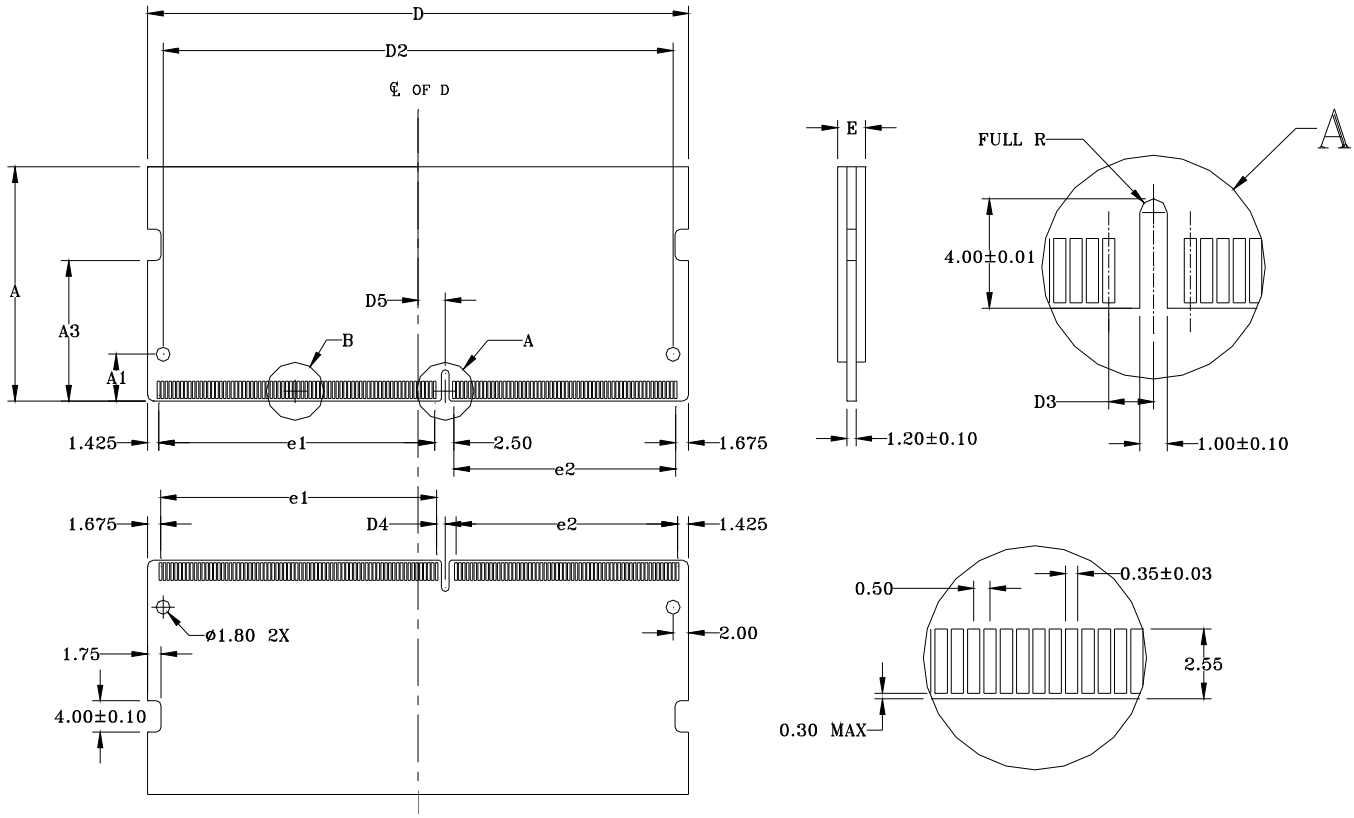
Pin	Name	Pin	Name	Pin	Name	Pin	Name
117	V_{DD}	118	V_{DD}	247	V_{SS}	248	V_{SS}
119	A12	120	A11	249	D58	250	D59
121	A9	122	A7	251	V_{SS}	252	V_{SS}
123	V_{DD}	124	V_{DD}	253	SCL	254	SDA
125	A8	126	A5	255	V_{DDSPD}	256	SA0
127	A6	128	A4	257	V_{PP}	258	V_{TT}
129	V_{DD}	130	V_{DD}	259	V_{PP}	260	SA1

Table 7 - Pin Description

Pin Name	Description	Pin Name	Description
V_{DD}	SDRAM I/O & core power supply	V_{PP}	SDRAM activating power supply
V_{REFCA}	SDRAM command/address reference supply	V_{SS}	Power supply return (ground)
A0-A15	SDRAM address bus	BA0-BA1	SDRAM bank select
BG0	SDRAM bank group select	CKE0	SDRAM clock enable lines
ODT0	SDRAM on-die termination contorl lines	/WE	SDRAM write enable
/CAS	SDRAM column address strobe	/RAS	SDRAM row address strobe
/CS0	Rank Select lines	/ACT	SDRAM activate
CK0-CK1	SDRAM clocks (positive line of differential pair)	/CK0-/CK1	SDRAM clocks (negative line of differential pair)
D0-D63	DIMM memory data bus	/DM0-/DM7 /DBI0-/DBI7	SDRAM data masks/data bus inversion
DQS0-DQS7	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS7	SDRAM data strobes (negative line of differential pair)
PARITY	SDRAM parity input	SDA	EEPROM data line
SCL	EEPROM bus clock	/ALERT	SDRAM /ALERT
SA0-SA2	SDRAM address input	V_{TT}	SDRAM I/O termination supply
/RESET	Set SDRAMs to a known state	V_{DDSPD}	EERPOM positive power supply
NC	Spare pins (no connect)	-	-

Module Dimension

Figure 1 – 260 Pin DDR4 Unbuffered SO-DIMM



Symbol	MIN	NOM	MAX
A	29.85	30.00	30.15
A1		6.00 Basic	
A3	17.85	18.00	18.15
D	69.45	69.60	69.75
D2		65.60 Basic	
D3		1.375 Basic	
D4		1.125 Basic	
D5		3.50 Basic	
e1		35.50 Basic	
e2		28.50 Basic	
E			3.70

Notes:

1 All dimensioning and tolerancing conform to ASME Y14.5M–1994.
2 Tolerance on all dimensions ± 0.15 unless otherwise specified.
3 All dimensions are in millimeters.

Revision History

Revision	Descriptions	Release Date
1.0	Initial release	May, 2022