Product Specification | Rev. 1.0 | 2015

IMM64M72SDDUD8AG (Die Revision B)
512MByte (64M x 72 Bit)

512MB SDRAM ECC Unbuffered DIMM
RoHS Compliant Product

Version: Rev. 1.0, JUN 2015

1.0 - Initial release

Remark:
Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures .

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: sales@intelligentmemory.com

Features

- 168-Pin Unbuffered Dual-In-Line Memory Module
- Capacity: 512MB
- Power Supply: VDD, VDDQ = 3.3± 0.3 V
- 72 Bit Data Bus Width with ECC
- Programmable CAS Latency (CL):
  - PC133: 2, 3
  - PC100: 2
- Input/Output Data Masking
- Burst Mode Operation
- Burst Type (Sequential & Interleave)
- Burst Length: 1, 2, 4, 8 or Full page
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Serial Presence Detect (SPD) with EEPROM
- Single Sided Components
- 100% RoHS-Compliant
- Gold Edge Contacts
- Standard Module Height: 34.93mm (1.375 inch)

Table 1 - Ordering Information for RoHS Compliant Product				
Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM64M72SDDUD8AG-Bzzzy	512MB	64Mx72	2	512MB SDR Unbuffered DIMM

Notes:
y: Operating Temperature
zzz: Speed Grade

Table 2 - Temperature Grade		
Part Number	Temperature Grade	T_a
Blank	Commercial temperature	0°C to 70°C
I	Industrial temperature	-40°C to 85°C

Table 3 - Speed Grade		
Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
75	PC133	133MHz (7.5ns@CL=3)
10	PC100	100MHz (10ns@CL=2)

Table 4 - Memory Chip Information					
Part Number	Base Device Brand	Base Device	Voltage	Type	Chip Packing
IMM64M72SDDUD8AG-Bzzzy	I'M	IM2508SDBBTG	3.3V	32Mx8	Lead Free

Part Number Decoder

IMM 64M72 SD DU D 8 A G - B 75 (I)

Intelligent Memory Module

Module Configuration
64M72 = 64Mx72 (512MB)

Memory Type
SD = SDRAM

Module Form-Factor
DU = Unbuffered DIMM

Number of Ranks
D = Dual Rank

DRAM Bit width
8 = using x8 components

Module PCB Revision
A = Revision A
B = Revision B
C = Revision C

RoHS compliance
G = Green / RoHS

IC Revision
A = Revision A
B = Revision B
C = Revision C
D = Revision D

Speed Grade
75 = PC133
10 = PC100

Temperature Grade
Blank = Commercial Temperature (0°C to 70°C T_a)
I = Industrial Temperature (-40°C to 85°C T_a)

Table 5 – Addressing

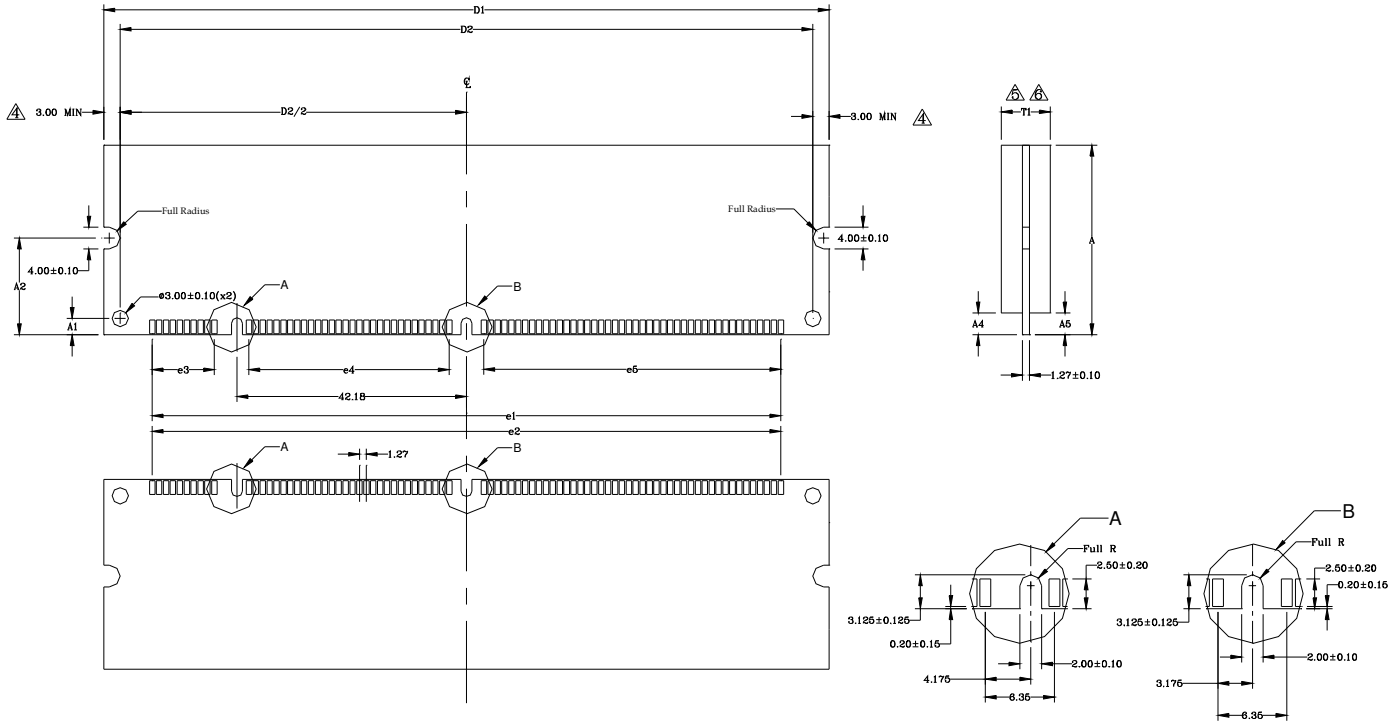
Parameter	512MB
Refresh count	8K
Row address	8K A[12:0]
Device bank address	4 BA[1:0]
Device configuration	256Mb (32Mx8)
Column address	1K A[9:0]
Module rank address	4 /S[3:0]
Number of devices	18

Table 6 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VSS	85	VSS	43	VSS	127	VSS
2	D0	86	D32	44	NC	128	CKE0
3	D1	87	D33	45	/S2	129	/S3
4	D2	88	D34	46	DQM2	130	DQM6
5	D3	89	D35	47	DQM3	131	DQM7
6	VDD	90	VDD	48	NC	132	NC
7	D4	91	D36	49	VDD	133	VDD
8	D5	92	D37	50	NC	134	NC
9	D6	93	D38	51	NC	135	NC
10	D7	94	D39	52	CB2	136	CB6
11	D8	95	D40	53	CB3	137	CB7
12	VSS	96	VSS	54	VSS	138	VSS
13	D9	97	D41	55	D16	139	D48
14	D10	98	D42	56	D17	140	D49
15	D11	99	D43	57	D18	141	D50
16	D12	100	D44	58	D19	142	D51
17	D13	101	D45	59	VDD	143	VDD
18	VDD	102	VDD	60	D20	144	D52
19	D14	103	D46	61	NC	145	NC
20	D15	104	D47	62	NC	146	NC
21	CB0	105	CB4	63	CKE1	147	NC
22	CB1	106	CB5	64	VSS	148	VSS
23	VSS	107	VSS	65	D21	149	D53
24	NC	108	NC	66	D22	150	D54
25	NC	109	NC	67	D23	151	D55
26	VDD	110	VDD	68	VSS	152	VSS
27	/WE	111	/CAS	69	D24	153	D56
28	DQM0	112	DQM4	70	D25	154	D57
29	DQM1	113	DQM5	71	D26	155	D58
30	/S0	114	/S1	72	D27	156	D59
31	NC	115	/RAS	73	VDD	157	VDD
32	VSS	116	VSS	74	D28	158	D60
33	A0	117	A1	75	D29	159	D61
34	A2	118	A3	76	D30	160	D62
35	A4	119	A5	77	D31	161	D63
36	A6	120	A7	78	VSS	162	VSS
37	A8	121	A9	79	CK2	163	CK3
38	A10, AP	122	BA0	80	NC	164	NC
39	BA1	123	A11	81	NC	165	SA0
40	VDD	124	VDD	82	SDA	166	SA1
41	VDD	125	CK1	83	SCL	167	SA2
42	CK0	126	A12	84	VDD	168	VDD

Table 7 - Pin Description			
Pin Name	Description	Pin Name	Description
VDD	SDRAM positive power supply	VSS	Power supply return (Ground)
CK0-CK3	Clock Input	CKE0,CKE1	Clock enable
A0-A12	Address Input	BA0-BA1	SDRAM bank address
D0-D63	DIMM memory data bus	DQM0-DQM7	Data input or output mask
CB0-CB7	Data check bits input/output	/S0-/S3	Chip select
/RAS	Row address strobe	/WE	Write enable
/CAS	Column address strobe	SCL	EEPROM clock input
SDA	EEPROM data input or output	SA0-SA2	EEPROM slave address select
NC	Spare Pins (no connect)		

Figure 1 –Module Dimension 168 Pin SDRAM Unbuffered DIMM



Symbol	MIN	NOM	MAX
A	34.795	34.925	35.055
A1		3.00BSC	
A2		17.80BSC	
A4	4.00		
A4	4.00		
D1	133.20	133.35	133.50
D2		127.35BSC	
e1		115.57BSC	
e2		115.57BSC	
e3		11.43BSC	
e4		36.83BSC	
e5		54.61BSC	
A4			4.00

Notes:

1 All dimensioning and tolerancing conform to ASME Y14.5M–1994.
2 Tolerances on all dimensions ± 0.13 unless otherwise specified.
3 All dimensions are in millimeters.
4 3.00mm minimum applies to both 4.00mm wide notch length and component keepout area.
5 Dimension applicable when components mounted on both sides.
6 When SOJ devices are used for assembly of this module, the maximum thickness overall shall not exceed 9.00mm. When the TSOP devices are used, the maximum thickness shall not exceed 4.00mm.