IME8G32D4GAB

PRELIMINARY

8Gbit DDR4 SDRAM with integrated ECC error correction

8 BANKS X 32Mbit X 32

Ordering Speed Code	- 083	- 075	- 062
	DDR4-2400	DDR4-2666	DDR4-3200
Clock Cycle Time ($t_{CK10,\ CWL=9}$)	1.5 ns	1.5 ns	1.5 ns
Clock Cycle Time ($t_{CK11,\ CWL=9,11}$)	1.25 ns	1.25 ns	1.25 ns
Clock Cycle Time ($t_{CK12,\ CWL=9,11}$)	1.25 ns	1.25 ns	1.25 ns
Clock Cycle Time ($t_{CK13,\ CWL=10,12}$)	1.071 ns	1.071 ns	1.071 ns
Clock Cycle Time ($t_{CK14,\ CWL=10,12}$)	1.071 ns	1.071 ns	1.071 ns
Clock Cycle Time ($t_{CK15,\ CWL=11,14}$)	0.935 ns	0.938 ns	0.938 ns
Clock Cycle Time ($t_{CK16,\ CWL=11,14}$)	0.938 ns	0.938 ns	0.938 ns
Clock Cycle Time ($t_{CK17,\ CWL=12,16}$)	0.833 ns	0.833 ns	0.833 ns
Clock Cycle Time ($t_{CK18,\ CWL=12,16}$)	0.833 ns	0.833 ns	0.833 ns
Clock Cycle Time ($t_{CK19,\ CWL=14,18}$)	-	0.750 ns	0.750 ns
Clock Cycle Time ($t_{CK20,\ CWL=14,18}$)	-	-	0.750 ns
Clock Cycle Time ($t_{CK22,\ CWL=16,20}$)	-	-	0.625 ns
System Frequency ($f_{CK\ max}$)	1200 MHz	1333 MHz	1600 MHz

Specifications

- Density : 8Gbits
- Organization :
  - 32M words x 32 bits x 8 banks
- Package :
  - 144-ball FBGA
  - Lead-free
- Power supply (JEDEC standard 1.2V)
  - VDD = 1.2V ± 5%
  - VPP = 2.375V to 2.75V
- Data rate : 2400Mbps/ 2666Mbps/ 3200Mbps
- 8 internal banks
  - 8 banks (4 banks x 2 bank groups) for x32 product
- Interface: Pseudo Open Drain (POD)
- Burst lengths (BL) : 8 and 4 with Burst Chop (BC)
- $\overline{\text{CAS}}$ Latency (CL) : 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 22
- $\overline{\text{CAS}}$ Write Latency (CWL) : 9, 10, 11, 12, 14, 16, 18, 20
- On-Die Termination (ODT): nom. Values of RZQ/7, RZQ/5 (RZQ = 240Ω)
- Precharge : auto precharge option for each burst access
- Refresh : auto-refresh, self-refresh
- Refresh cycles :
  - Average refresh period
    7.8 µs at 0°C ≤ Tc ≤ +85°C
    3.9 µs at +85°C < Tc ≤ +95°C
- Operating case temperature range
  - Commercial Tc = 0°C to +95°C
  - Industrial Tc = -40°C to +95°C

*Option*Marking

- Configuration
  - ●256Mx32 (8 Banks x 32Mbits x32) — 8G32
- Package
  - ●144-ball FBGA (11.5mm x 15.5mm) — B
- Leaded/Lead-free
  - ●Leaded — <blank>
  - ●Lead-free/RoHS — G
- Speed/Cycle Time
  - ●0.625ns @ CL22 (DDR4-3200) — -062
  - ●0.750ns @ CL19 (DDR4-2666) — -075
  - ●0.833ns @ CL17 (DDR4-2400) — -083
- Temperature
  - ●Commercial 0°C to 95°C Tc — <blank>
  - ●Industrial -40°C to 95°C Tc — I

Example Part Number: IME8G32D4GABG-062I

Features

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipe-lined architecture
- Bi-directional differential data strobe (DQS and $\overline{DQS}$) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{CK}$)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Write Cyclic Redundancy Code (CRC) for DQ error detect and inform it to controller during high-speed operation
- Data Bus Inversion (DBI)
  - Improve the power consumption and signal integrity of the memory interface
- Programmable preamble is supported both of 1tCK and 2tCK mode
- Command Address (CA) Parity for command/address signal error detect and inform it to controller
- VREFDQ training
  - VREFDQ generate inside DRAM and further train per DRAM
- Per DRAM Addressability (PDA)
  - Each DRAM can be set a different mode register value individually and has individual adjustment
- Fine granularity refresh
  - 2x, 4x mode for smaller tRFC
- Maximum power saving mode for the lowest power consumption with no internal refresh activity
- Programmable Partial Array Self-Refresh (PASR)
- $\overline{RESET}$ pin for Power-up sequence and reset function

Special Features(ECC – Functionality)

- Embedded error correction code (ECC) functionality corrects single bit errors within each 64 bit memory-word.
- The error correction is performed automatically inside the ECC DRAM device.
- Parity data is generated by an internal ECC logic and then stored in additional, dedicated memory space.
- Fully compatible to JEDEC standard DRAM operation and timings.
- JEDEC compliant FBGA package (drop in replacement).

ECC – Functionality / Challenges and Achievements

During the production test, the ECC DRAMs are verified to pass extensive burn-in, core-function and speed tests throughout the complete memory array, including the memory-space for the parity-data. Only when every single memory cell has passed these tests, the ECC function is switched on by hardware and the products get shipped. With the ECC function activated, customers will have unparalleled functionality and quality.

Embedded ECC functionality

Intelligent Memory ECC DRAMs are JEDEC compliant components with integrated error-correction. The internal logic automatically detects and corrects single-bit-errors "on the fly" without any delays or additional latencies compared to conventional DRAM components. ECC DRAMs have additional memory-space to store the ECC-check-bits. Internally, the ECC DRAM works with a 72 bit wide buffer. When writing to the DRAM, an additional 8 ECC check-bits are being generated per each 64 bit data-word. Upon a Read-command, the whole 64+8 bit word is transferred to the buffer and automatically corrected by an ECC Hamming Code (72, 64). The corrected data is then applied to the DQ lines of the ECC DRAM in bit-widths of 4, 8, 16 or 32 bit, depending on the organization of the device.

The ECC algorithm is able to detect and correct one bit-error per 64+8 bit data-word. A 1 Gigabit ECC DRAM component has 16,777,216 data-words of 64 Bits. In each of these data-words, one single-bit error could be corrected, resulting in approximately 16 million times higher reliability of ECC DRAM compared to a conventional DRAM with similar capacity.

Note: If Burst Length x DRAM-I/O-width < 64 bit during a Write-command, the ECC-functionality is limited. Please contact Intelligent Memory for further details.

Comparison to conventional ECC implementation

ECC error correction is very common on high end industrial applications and servers. It normally requires an ECC-capable memory-controller which has an extra-wide data-bus with for example 72 bits (64 data-bits + 8 check-bits). The memory controller generates the required additional check-bits for the data and writes the extra wide data-word to the memory. Upon a Read-command, the memory controller will verify the data-integrity of the data-word + check-bits and performs the correction algorithm. Performing this algorithm affects the systems performance. In addition to the requirement for an ECC-capable memory controller, the conventional way of ECC correction requires multiple DRAMs to be accessed in parallel to achieve the extra-wide bit-width. On Server-memory-modules, for example, 18 DRAM-components with 4 data-lines each are put in parallel to reach the total 72 bit extra-wide data-bus.

With IM ECC DRAM, the check-bit-generation, verification and correction is performed inside the memory device. Every single ECC DRAM performs the error correction by itself, thus it does not require ECC-capable processors/controllers nor any wide data-bus between the controller and the DRAM. Because the ECC DRAM components are JEDEC compliant, they are drop-in replacements to conventional DRAM-memory. Any existing application that is currently built with conventional DRAM can be equipped with error-correction functionality. Note that, if a standard 64 bit memory-module is built using ECC DRAMs, the depth of error-correction is deeper than on 72 bit ECC memory module as each DRAM component on the module performs its own ECC correction-algorithm.

Why is ECC error correction important?

Numerous analyzes and field-studies have proven DRAM single-bit errors to be the root cause of system-malfunctions or data-corruptions.

According to the field-study by the University Of Toronto called "DRAM Errors In The Wild – A Large-Scale field study", 25000 to 70000 ECC correctable single-bit errors occur per Megabit of DRAM within 1 billion hours of operation.

While not every single bit error causes a system crash, the application-software may become unstable or important data can be altered and the wrong data can pass through to external media, resulting in unrecoverable data-errors.

While all DRAMs are factory-tested by long burn-in-testing and effective functional and speed testing with different patterns and voltage variations, single-bit errors are technically not avoidable.

The effects are typically transient and difficult-to-repeat single data-bit flips. Many of these single-bit errors appear only under heavy stress or longer time of use of the DRAM, resulting as random system malfunctions or data-corruptions of the application. After a reset, the systems work again until the next occurrence of a single bit error reappears. It is difficult to prove a defect, as it is only a random effect which shows up in different ways at unknown times.

ECC corrects the output, but not the content of the Memory Array. For maximum stability we recommend to do periodical "scrubbing" (read and overwrite)

Possible root-causes for single-bit errors

DRAM cells consist of capacitors holding an electric charge which defines if the memory-cell contains a logical 0 or 1. These capacitor-cells are switched by transistors.

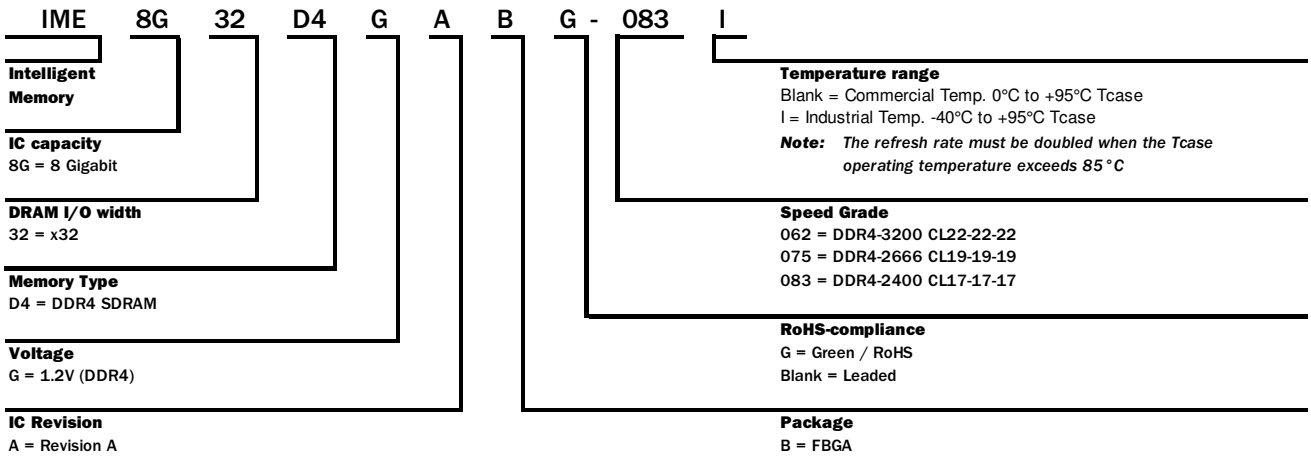
With the trend to smaller process technologies, higher speeds and lower supply-voltages, DRAM memory cells become more sensitive to noise on the signals, electromagnetic fields, cosmic rays or particle radiation. Also power peaks and variations in the signal-timing can cause single-bit errors.

Furthermore, depending on the age and intensity of use of those DRAM components, memory-cells suffer from various degrees of degradation. The isolation of the capacitors gets reduced and leakage increases, leading to lower data-retention-times of some cells. As data-retention times approach the refresh-times, data-bit tend to sometimes show up an incorrect binary value. The effects often appear only with certain data-patterns, at specific temperatures or at high data-traffic to the DRAM. The cell gets "weak", but the errors in the cell are not easily repeatable as they are not permanent.

There is no way to improve the DRAM technology itself, except by going back to larger processes, lower speeds and higher voltages. Pre-Testing the DRAMs longer, with more stress and wider guardbands, or even with automotive certified screening-processes does not fully protect from the risk of single-bit errors.

The only practical way to avoid single-bit errors is to use error correction algorithms such as ECC.

Part Number Information



Pin Configurations

144-ball FBGA (x32 configuration)

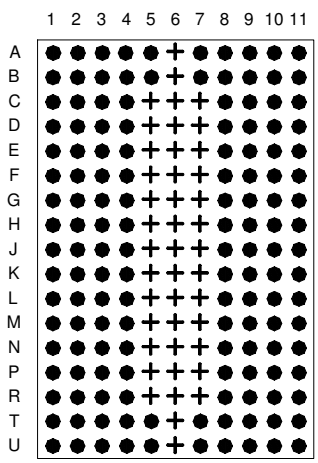
	1	2	3	4	5	6	7	8	9	10	11	
A	VPP	VDDQ	DQS0	$\overline{\text{DQS0}}$	VDDQ		VDDQ	$\overline{\text{DQS1}}$	DQS1	VDDQ	VDD	A
B	VSS	VSSQ	DQ0	$\overline{\text{DM0}}$ /$\overline{\text{DBI0}}$	VSSQ		VSSQ	DQ8	DQ9	VSSQ	VSS	B
C	VDD	DQ3	DQ2	DQ1				DQ10	DQ11	DQ12	VDDQ	C
D	VDDQ	DQ4	DQ5	VSSQ				VSSQ	DQ13	DQ15	VSSQ	D
E	VSSQ	DQ6	DQ7	VDDQ				VDDQ	DQ14	$\overline{\text{DM1}}$ /$\overline{\text{DBI1}}$	ZQ	E
F	VDD	NC	VDDQ	ODT				CK	VDDQ	NC	VDD	F
G	VDD	NC	VSS	CKE				$\overline{\text{CK}}$	VSS	TEN	VDD	G
H	VREFCA	BA0	$\overline{\text{ACT}}$	$\overline{\text{WE}}$ /A14				$\overline{\text{CS}}$	$\overline{\text{RAS}}$ /A16	BA1	NC	H
J	VSS	A4	VSS	BG0				$\overline{\text{CAS}}$ /A15	VSS	A3	VSS	J
K	$\overline{\text{RESET}}$	A6	A0	A10/AP				A12/$\overline{\text{BC}}$	NC	A5	$\overline{\text{ALERT}}$	K
L	VDD	A8	VSS	A2				A1	VSS	A7	VDD	L
M	VDD	A11	VDDQ	PAR				A9	VDDQ	A13	VDD	M
N	NC	$\overline{\text{DM3}}$ /$\overline{\text{DBI3}}$	DQ30	VDDQ				VDDQ	DQ23	DQ22	VSSQ	N
P	VSSQ	DQ31	DQ29	VSSQ				VSSQ	DQ21	DQ20	VDDQ	P
R	VDDQ	DQ28	DQ27	DQ26				DQ17	DQ18	DQ19	VDD	R
T	VSS	VSSQ	DQ25	DQ24	VSSQ		VSSQ	$\overline{\text{DM2}}$ /$\overline{\text{DBI2}}$	DQ16	VSSQ	VSS	T
U	VDD	VDDQ	DQS3	$\overline{\text{DQS3}}$	VDDQ		VDDQ	$\overline{\text{DQS2}}$	DQS2	VDDQ	VPP	U

Ball Locations

● Populated ball
✚ Ball not populated

Top view

(See the balls through the package)



Signal Pin Description

Pin	Type	Function
A0 – A13	Input	Address inputs A10/AP: Auto precharge A12/$\overline{BC}$: Burst chop
BA0 – BA1	Input	Bank select
BG0	Input	Bank group input
DQ0 – DQ31	Input/ Output	Data input/output
DQS0 – DQS3 $\overline{DQS0}$ – $\overline{DQS3}$	Input/ Output	Differential data strobe
$\overline{CS}$	Input	Chip select
$\overline{RAS}$/A16 $\overline{CAS}$/A15 $\overline{WE}$/A14	Input	Command input
$\overline{ACT}$	Input	Activation command input
CKE	Input	Clock enable
CK, $\overline{CK}$	Input/ Output	Differential clock input
$\overline{DM0}$ – $\overline{DM3}$	Input/ Output	Write data mask
$\overline{DBI0}$ – $\overline{DBI3}$	Input/ Output	Data bus inversion
ODT	Input	ODT control
$\overline{RESET}$	Input	Active low asynchronous reset
PAR	Input/ Output	Command and address parity
$\overline{ALERT}$	Input/ Output	Alert
VDD	Supply	Supply voltage for internal circuit
VSS	Supply	Ground for internal circuit
VDDQ	Supply	Supply voltage for DQ circuit
VSSQ	Supply	Ground for DQ circuit
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference pin for ZQ calibration
NC		No connection
TEN		Connectivity test mode enable

Standard Speed Bins

DDR4-2400 Speed Bins

Speed Bin				-083 (DDR4-2400)		Unit	Notes
CL-nRCD-nRP				17-17-17			
Parameter			Symbol	Min	Max		
Internal read command to first data			tAA	14.16[14] (13.75)[5,12]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min)+ 3nCK	tAA(max)+ 3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.16 (13.75)[5,12]	-	ns	12
PRE command period			tRP	14.16 (13.75)[5,12]	-	ns	12
ACT to PRE command period			tRAS	32	9 * tREFI	ns	12
ACT to ACT or PRE command time			tRC	46.16 (45.75)[5,12]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(avg)	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(avg)	1.5	1.6	ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(avg)	Reserved		ns	4
	CL = 11	CL = 13	tCK(avg)	1.25	<1.5	ns	1,2,3,4,8
				(Optional)[5,12]			
	CL = 12	CL = 14	tCK(avg)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(avg)	Reserved		ns	4
	CL = 13	CL = 15	tCK(avg)	1.071	<1.25	ns	1,2,3,4,8
				(Optional)[5,12]			
	CL = 14	CL = 16	tCK(avg)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(avg)	Reserved		ns	4
	CL = 15	CL = 18	tCK(avg)	0.938	<1.071	ns	1,2,3,4,8
				(Optional)[5,12]			
	CL = 16	CL = 19	tCK(avg)	0.938	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(avg)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(avg)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(avg)	0.833	<0.938	ns	
	CL = 18	CL = 21	tCK(avg)	0.833	<0.938	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18		nCK	13
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21		nCK	
Supported CWL settings				9,10,11,12,14,16		nCK	

DDR4-2666 Speed Bins

Speed Bin				-075 (DDR4-2666)		Unit	Notes
CL-nRCD-nRP				19-19-19			
Parameter			Symbol	Min	Max		
Internal read command to first data			tAA	14.25[14] (13.75)[5,12]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min)+ 3nCK	tAA(max)+ 3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.25 (13.75)[5,12]	-	ns	12
PRE command period			tRP	14.25 (13.75)[5,12]	-	ns	12
ACT to PRE command period			tRAS	32	9 * tREFI	ns	12
ACT to ACT or PRE command time			tRC	46.25 (45.75)[5,12]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(avg)	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(avg)	1.5	1.6	ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(avg)	Reserved		ns	4
	CL = 11	CL = 13	tCK(avg)	1.25	<1.5	ns	1,2,3,4,8
				(Optional)[5,12]			
	CL = 12	CL = 14	tCK(avg)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(avg)	Reserved		ns	4
	CL = 13	CL = 15	tCK(avg)	1.071	<1.25	ns	1,2,3,4,8
				(Optional)[5,12]			
	CL = 14	CL = 16	tCK(avg)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(avg)	Reserved		ns	4
	CL = 15	CL = 18	tCK(avg)	0.938	<1.071	ns	1,2,3,4,8
				(Optional)[5,12]			
	CL = 16	CL = 19	tCK(avg)	0.938	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(avg)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(avg)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(avg)	0.833	<0.938	ns	
	CL = 18	CL = 21	tCK(avg)	0.833	<0.938	ns	1,2,3
CWL = 14,18	CL = 17	CL = 20	tCK(avg)	Reserved		ns	4
	CL = 18	CL = 21	tCK(avg)	Reserved		ns	4
	CL = 19	CL = 22	tCK(avg)	0.750	<0.833	ns	1,2,3,8
	CL = 20	CL = 23	tCK(avg)	0.750	<0.833	ns	1,2,3,8
Supported CL Settings				10,11,12,13,14,15,16,17,18,19,20		nCK	13
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21,22,23		nCK	
Supported CWL settings				9,10,11,12,14,16,18		nCK	

DDR4-3200 Speed Bins

Speed Bin				-062 (DDR4-3200)		Unit	Notes
CL-nRCD-nRP				22-22-22			
Parameter			Symbol	Min	Max		
Internal read command to first data			tAA	13.75[14]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min)+ 3nCK	tAA(max)+ 3nCK	ns	12
ACT to internal read or write delay time			tRCD	13.75	-	ns	12
PRE command period			tRP	13.75	-	ns	12
ACT to PRE command period			tRAS	32	9 * tREFI	ns	12
ACT to ACT or PRE command time			tRC	45.75	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(avg)	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(avg)	1.5	1.6	ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(avg)	Reserved		ns	4
	CL = 11	CL = 13	tCK(avg)	1.25	<1.5	ns	1,2,3,4,8
				(Optional)[5,12]			
	CL = 12	CL = 14	tCK(avg)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(avg)	Reserved		ns	4
	CL = 13	CL = 15	tCK(avg)	1.071	<1.25	ns	1,2,3,4,8
				(Optional)[5,12]			
	CL = 14	CL = 16	tCK(avg)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(avg)	Reserved		ns	4
	CL = 15	CL = 18	tCK(avg)	0.938	<1.071	ns	1,2,3,4,8
				(Optional)[5,12]			
	CL = 16	CL = 19	tCK(avg)	0.938	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(avg)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(avg)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(avg)	0.833	<0.938	ns	
	CL = 18	CL = 21	tCK(avg)	0.833	<0.938	ns	1,2,3
CWL = 14,18	CL = 17	CL = 20	tCK(avg)	Reserved		ns	4
	CL = 18	CL = 21	tCK(avg)	Reserved		ns	4
	CL = 19	CL = 22	tCK(avg)	0.750	<0.833	ns	1,2,3,8
	CL = 20	CL = 23	tCK(avg)	0.750	<0.833	ns	1,2,3,8
CWL = 16,20	CL = 20	CL = 24	tCK(avg)	Reserved		ns	4
	CL = 21	CL = 24	tCK(avg)	Reserved		ns	4
	CL = 22	CL = 26	tCK(avg)	0.625	<0.750	ns	1,2,3,8
Supported CL Settings				10,11,12,13,14,15,16,17,18,19,20,22		nCK	13
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21,22,23,26		nCK	
Supported CWL settings				9,10,11,12,14,16,18		nCK	

Speed Bin Table Notes

Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case
- DDR4-1600, 1866, 2133 and 2400 Speed Bin Tables are valid only when Geardown Mode is disabled

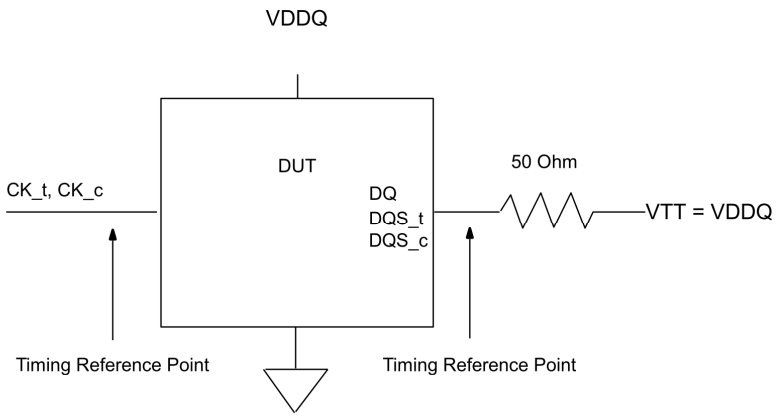
1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.938 or 0.833 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns). This result is tCK(avg). MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Reserved for DDR4-2666 speed bin.
10. Reserved for DDR4-3200 speed bin.
11. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
12. Parameter apply from tCK(avg)min to tCH(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
13. CL number in parentheses, it means that these numbers are optional.

Electrical Characteristics & AC Timing

Reference Load for AC Timing and Output Slew Rate

Below figure represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



Reference Load for AC Timing and Output Slew Rate

tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined as shown in the table.

tREFI by device density

Parameter	Symbol		8Gb	Units
Average periodic refresh interval	tREFI	0℃ ≤ TCASE ≤ 85℃	7.8	µs
		85℃ ≤ TCASE ≤ 95℃	3.9	µs

Timing Parameters by Speed Grade

Timing Parameters by Speed Bin for DDR4-2400 to DDR4-3200

Parameter	Symbol	- 083 (DDR4-2400)		- 075 (DDR4-2666)		- 062 (DDR4-3200)		Unit
		Min	Max	Min	Max	Min	Max	
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	ns
Average Clock Period	tCK(avg)	0.833	<0.938	0.75	<0.833	0.625	<0.75	ns
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)
Clock Period Jitter- total	JIT(per)_tot	-42	42	-38	38	-32	32	ps
Clock Period Jitter- deterministic	JIT(per)_dj	-21	21	-19	19	-16	16	ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-33	33	-30	30	-25	25	ps
Cycle to Cycle Period Jitter	tJIT(cc)_dj	83		75		62		ps
Cycle to Cycle Period Jitter deterministic	tJIT(cc)_dj	42		38		32		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	67		60		50		ps
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cumulative error across 2 cycles	tERR(2per)	-61	61	-55	55	-46	46	ps
Cumulative error across 3 cycles	tERR(3per)	-73	73	-66	66	-55	55	ps
Cumulative error across 4 cycles	tERR(4per)	-81	81	-73	73	-61	61	ps
Cumulative error across 5 cycles	tERR(5per)	-87	87	-78	78	-65	65	ps
Cumulative error across 6 cycles	tERR(6per)	-92	92	-83	83	-69	69	ps
Cumulative error across 7 cycles	tERR(7per)	-97	97	-87	87	-73	73	ps
Cumulative error across 8 cycles	tERR(8per)	-101	101	-91	91	-76	76	ps
Cumulative error across 9 cycles	tERR(9per)	-104	104	-94	94	-78	78	ps
Cumulative error across 10 cycles	tERR(10per)	-107	107	-96	96	-80	80	ps
Cumulative error across 11 cycles	tERR(11per)	-110	110	-99	99	-83	83	ps
Cumulative error across 12 cycles	tERR(12per)	-112	112	-101	101	-84	84	ps
Cumulative error across 13 cycles	tERR(13per)	-114	114	-104	104	-88	88	ps
Cumulative error across 14 cycles	tERR(14per)	-116	116	-106	106	-89	89	ps
Cumulative error across 15 cycles	tERR(15per)	-118	118	-108	108	-91	91	ps
Cumulative error across 16 cycles	tERR(16per)	-120	120	-110	110	-92	92	ps
Cumulative error across 17 cycles	tERR(17per)	-122	122	-111	111	-94	94	ps
Cumulative error across 18 cycles	tERR(18per)	-124	124	-113	113	-95	95	ps

Parameter	Symbol	- 083 (DDR4-2400)		- 075 (DDR4-2666)		- 062 (DDR4-3200)		Unit
		Min	Max	Min	Max	Min	Max	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) t ERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)						ps
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	62	-	TBD(55)	-	TBD(40)	-	ps
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	162	-	TBD(145)	-	TBD(130)	-	ps
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	87	-	TBD(80)	-	TBD(65)	-	ps
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	162	-	TBD(145)	-	TBD(130)	-	ps
Control and Address Input pulse width for each input	tIPW	410	-	TBD(385)	-	TBD(350)	-	ps
CAS_n to CAS_n command delay for same bank group	tCCD_L	Max(5nCK, 5.000ns)	-	Max(4nCK, 5ns)	-	Max(4nCK, 5ns)	-	nCK
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK, 3.3ns)	-	Max(4nCK, 3.0ns)	-	Max(4nCK, 2.5ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S (1/2K)	Max(4nCK, 3.3ns)	-	Max(4nCK, 3.0ns)	-	Max(4nCK, 2.5ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L (1/ 2K)	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	nCK
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	ns
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 21ns)	-	Max(20nCK, 21ns)	-	Max(20nCK, 21ns)	-	ns
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 13ns)	-	Max(16nCK, 12ns)	-	Max(16nCK, 10ns)	-	ns
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max (2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-	
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	
Internal READ Command to PRE-CHARGE Command delay	tRTP	Max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	
WRITE recovery time	tWR	15	-	15	-	15	-	ns
Write recovery time when CRC and DM are enabled	tWR_CRC _DM	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	ns

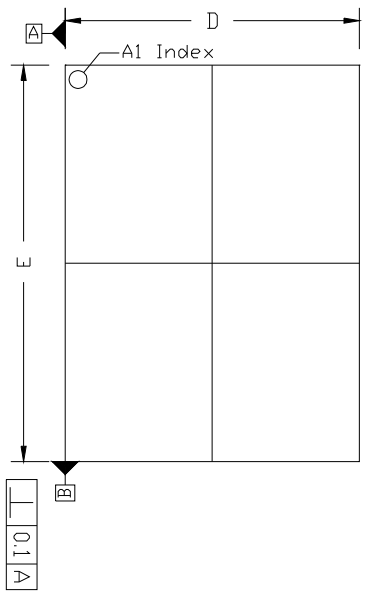
Parameter	Symbol	- 083 (DDR4-2400)		- 075 (DDR4-2666)		- 062 (DDR4-3200)		Unit
		Min	Max	Min	Max	Min	Max	
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+ max (5nCK, 3.75ns)	-	tWTR_S+ max (5nCK, 3.75ns)	-	tWTR_S+ max (5nCK, 3.75ns)	-	ns
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+ max (5nCK, 3.75ns)	-	tWTR_L+ max (5nCK, 3.75ns)	-	tWTR_L+ max (5nCK, 3.75ns)	-	ns
DLL locking time	tDLLK	768	-	854	-	1024	-	nCK
Mode Register Set command cycle time	tMRD	8	-	9	-	10	-	nCK
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	
Auto precharge write recovery + pre-charge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))						nCK
$\overline{CS}$ to Command Address Latency	tCAL	3	-	5	-	6	-	nCK
DQS, $\overline{DQS}$ to DQ skew, per group, per access	tDQSQ	-	TBD	-	TBD	-	TBD	tCK(avg) /2
DQ output hold time from DQS, $\overline{DQS}$	tQH	TBD	-	TBD	-	TBD	-	tCK(avg) /2
DQS, $\overline{DQS}$ differential READ Preamble(1 clock preamble)	tRPRE	0.9	TBD	0.9	TBD	0.9	TBD	tCK
DQS, $\overline{DQS}$ differential READ Preamble(2 clock preamble)	tRPRE	1.8	TBD	NA	NA	NA	NA	tCK
DQS, $\overline{DQS}$ differential READ Postamble	tRPST	0.33	TBD	0.33	TBD	0.33	TBD	tCK
DQS, $\overline{DQS}$ differential output high time	tQSH	0.4	-	0.4	-	0.4	-	tCK
DQS, $\overline{DQS}$ differential output low time	tQSL	0.4	0	0.4	-	0.4	-	tCK
DQS, $\overline{DQS}$ differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK
DQS, $\overline{DQS}$ differential WRITE Postamble	tWPST	0.33	TBD	0.33	TBD	0.33	TBD	tCK
DQS, $\overline{DQS}$ low-impedance time (Referenced from RL-1)	tLZ(DQS)	-300	150	-310	170	-250	160	ps
DQS, $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	150	-	170	-	160	ps
DQS, $\overline{DQS}$ differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	tCK
DQS, $\overline{DQS}$ differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	tCK
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK
DQS, $\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge	tDSS	0.18	-	0.18	-	0.18	-	tCK
DQS, $\overline{DQS}$ falling edge hold time from CK, $\overline{CK}$ rising edge	tDSH	0.18	-	0.18	-	0.18	-	tCK
DQS, $\overline{DQS}$ rising edge output timing locatino from rising CK, $\overline{CK}$ with DLL On mode	tDQSCK	-175	175	-170	170	-160	160	ps
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	

Parameter	Symbol	- 083 (DDR4-2400)		- 075 (DDR4-2666)		- 062 (DDR4-3200)		Unit
		Min	Max	Min	Max	Min	Max	
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	
Exit MPSM to commands not requiring a locked DLL	tXMP	TBD	-	TBD	-	TBD	-	
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	
CS setup time to CKE	tMPX_S	TBD	-	TBD	-	TBD	-	
CS hold time to CKE	tMPX_H	TBD	-	TBD	-	TBD	-	
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	nCK
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	nCK
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	nCK
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+ 10ns	-	tRFC(min)+ 10ns	-	tRFC(min)+ 10ns	-	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tX-S_ABORT (min)	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_ PAR	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max (5nCK,10ns)	-	max (5nCK,10ns)	-	max (5nCK,10ns)	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKS-RE_PAR	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max (5nCK,10ns)	-	max (5nCK,10ns)	-	max (5nCK,10ns)	-	
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	
Command pass disable delay	tCPDED	4nCK or 6ns	-	4nCK or 6ns	-	4nCK or 6ns	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	2	-	2	-	2	-	nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	2	-	2	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK

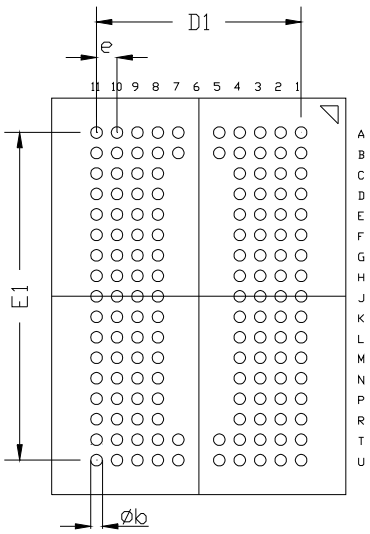
Parameter	Symbol	- 083 (DDR4-2400)		- 075 (DDR4-2666)		- 062 (DDR4-3200)		Unit
		Min	Max	Min	Max	Min	Max	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	2	-	2	-	2	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	ns
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
First DQS/$\overline{DQS}$rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	nCK
DQS/$\overline{DQS}$delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK
Write leveling setup time from rising CK, $\overline{CK}$ crossing to rising DQS/$\overline{DQS}$ crossing	tWLS	0.13	-	0.13	-	0.13	-	tCK(avg)
Write leveling hold time from rising DQS/$\overline{DQS}$crossing to rising CK, $\overline{CK}$ crossing	tWLH	0.13	-	0.13	-	0.13	-	tCK(avg)
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	ns
Write leveling output error	tWLOE	TBD						ns
Commands not guaranteed to be executed during this time	tPAR_UN-KNOWN	-	PL	-	PL	-	PL	
Delay from errant command to $\overline{ALERT}$assertion	tPAR_ALER-T_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	
Pulse width of $\overline{ALERT}$ signal when asserted	tPAR_ALER-T_PW	72	144	80	160	96	192	nCK
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALER-T_RSP	-	64	-	71	-	85	nCK
Parity Latency	PL	5		4		4		nCK
CRC error to $\overline{ALERT}$ latency	CRC_ALERT	3	13	3	13	3	13	ns
CRC $\overline{ALERT}$ pulse width	CRC_ALERT_PW	6	10	6	10	6	10	nCK
tRFC1 (min)	8Gb	350	-	350	-	350	-	ns
tRFC2 (min)	8Gb	260	-	260	-	260	-	ns
tRFC4 (min)	8Gb	160	-	160	-	160	-	ns

Package Diagram (x32)
144-Ball Fine Pitch Ball Grid Array Outline

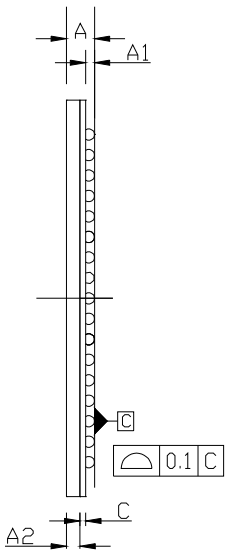
TOP VIEW



BOTTOM VIEW



SIDE VIEW



PKG outline

REF.	Dimension in mm		
	Min	Nom	Max
A	1.000	1.100	1.200
A1	0.300	0.350	0.400
A2	0.510	0.530	0.550
Øb	0.400	0.450	0.500
C	0.190	0.220	0.250
D	11.400	11.500	11.600
D1	8.000 BSC		
E	15.400	15.500	15.600
E1	12.800 BSC		
e	0.800 BSC		

Revision History

Rev	History	Release Date	Remark
0.1	Initial release	Jun. 2017	
0.2	Added ECC descriptions	Jul. 2017	
0.3	Added option for Industrial Temperature	Sep. 2017	