Product Specification | Rev. 1.0 | 2015

IMM128M72D1SOD8AG (Die Revision F)
1GByte (128M x 72 Bit)

1GB DDR Unbuffered SO-DIMM
RoHS Compliant Product

Version: Rev. 1.0, APR 2015

1.0 - Initial release

Remark:
Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures .

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Features

- 200-Pin Unbuffered Small Outline Dual-In-Line Memory Module
- Capacity: 1GB
- Power Supply:
  DDR 400: VDD, VDDQ = 2.6± 0.1 V
  DDR 333, 266: VDD, VDDQ = 2.5± 0.2 V
- Two Data Transfer per Clock Cycle
- Differential Clock Input (CK and /CK)
- 72 Bit Data Bus Width with ECC
- Programmable CAS Latency (CL):
  - PC-3200: 2.5, 3
  - PC-2700: 2.5
- Burst Type (Sequential & Interleave)
- Burst Length: 2, 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Serial Presence Detect (SPD) with EEPROM
- Double Sided Components
- 100% RoHS-Compliant
- Gold Edge Contacts
- Standard Module Height: 31.75mm (1.25 inch)

Table 1 - Ordering Information for RoHS Compliant Product				
Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM128M72D1SOD8AG-Fzzzy	1GB	128Mx72	2	1GB DDR Unbuffered SO-DIMM

Notes:
y: Operating Temperature
zzz: Speed Grade

Table 2 - Temperature Grade		
Part Number	Temperature Grade	T_a
Blank	Commercial temperature	0°C to 70°C
I	Industrial temperature	-40°C to 85°C

Table 3 - Speed Grade		
Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
5	PC3200	200MHz (5.0ns@CL=3)
6	PC2700	166MHz (6.0ns@CL=2.5)

Table 4 - Memory Chip Information					
Part Number	Base Device Brand	Base Device	Voltage	Type	Chip Packing
IMM128M72D1SOD8AG-Fzzzy	I'M	IM5108D1CFBG	2.5V	64Mx8	Lead Free

Part Number Decoder

IMM 128M72 D1 SO D 8 A G - F 5 (I)

Intelligent Memory Module

Module Configuration
128M72 = 128Mx72 (1GB)

Memory Type
D1 = DDR

Module Form-Factor
SO = Unbuffered SO-DIMM

Number of Ranks
D = Dual Rank

DRAM Bit width
8 = using x8 components

Module PCB Revision
A = Revision A
B = Revision B
C = Revision C

RoHS compliance
G = Green / RoHS

IC Revision
F = Revision F

Speed Grade
6 = PC-2700 / DDR-333
5 = PC-3200 / DDR-400

Temperature Grade
Blank = Commercial Temperature (0°C to 70°C T_a)
I = Industrial Temperature (-40°C to 85°C T_a)

Table 5 – Addressing

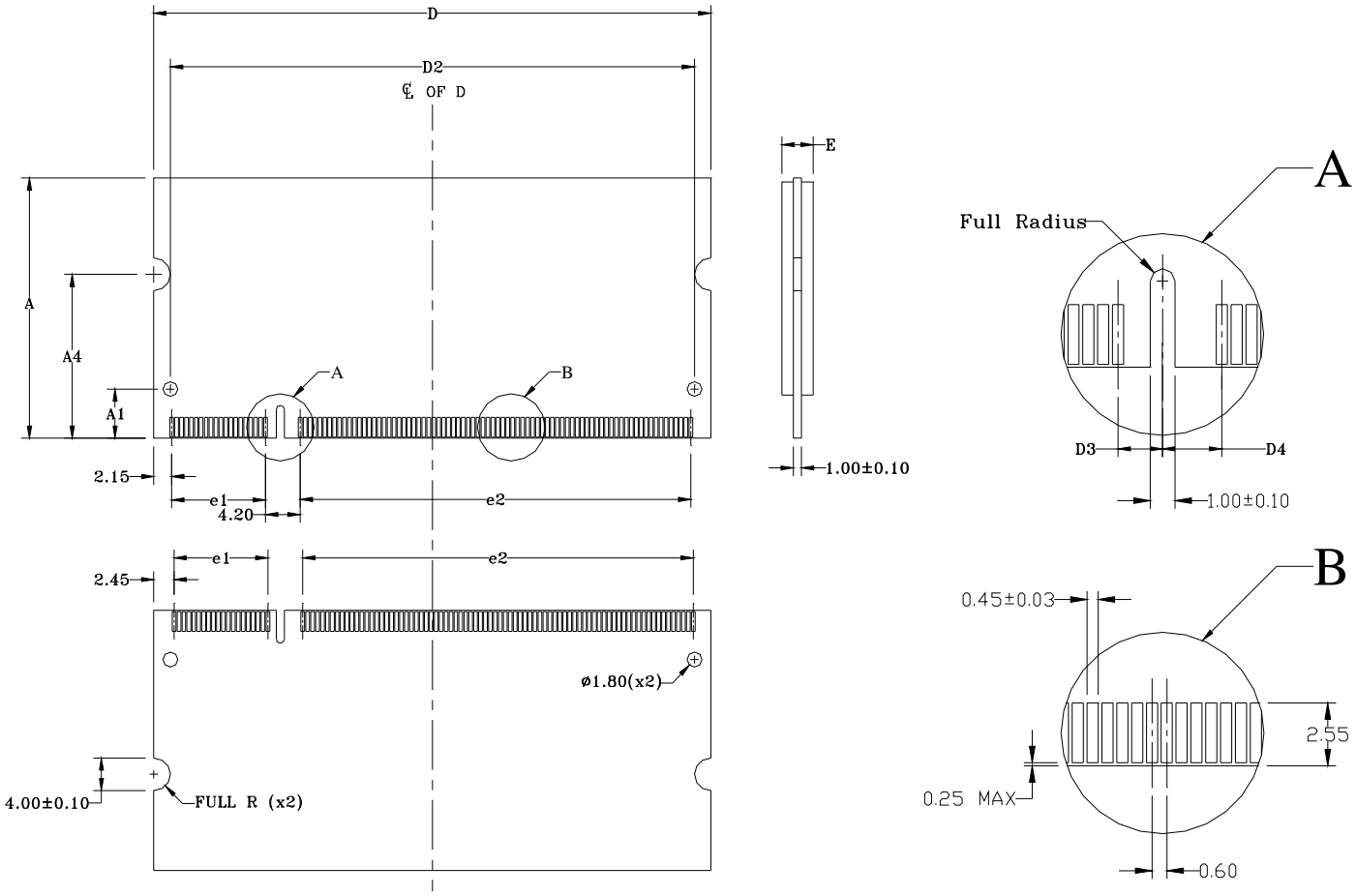
Parameter	1GB
Refresh count	8K
Row address	8K A[12:0]
Device bank address	4 BA[1:0]
Device configuration	512Mb (64Mx8)
Column address	2K A[9:0], A11
Module rank address	2 /S[1:0]
Number of devices	18

Table 6 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	2	VREF	101	A9	102	A8
3	VSS	4	VSS	103	VSS	104	VSS
5	D0	6	D4	105	A7	106	A6
7	D1	8	D5	107	A5	108	A4
9	VDD	10	VDD	109	A3	110	A2
11	DQS0	12	DM0	111	A1	112	A0
13	D2	14	D6	113	VDD	114	VDD
15	VSS	16	VSS	115	A10, AP	116	BA1
17	D3	18	D7	117	BA0	118	/RAS
19	D8	20	D12	119	/WE	120	/CAS
21	VDD	22	VDD	121	/S0	122	/S1
23	D9	24	D13	123	NC	124	NC
25	DQS1	26	DM1	125	VSS	126	VSS
27	VSS	28	VSS	127	D32	128	D36
29	D10	30	D14	129	D33	130	D37
31	D11	32	D15	131	VDD	132	VDD
33	VDD	34	VDD	133	DQS4	134	DM4
35	CK0	36	VDD	135	D34	136	D38
37	/CK0	38	VSS	137	VSS	138	VSS
39	VSS	40	VSS	139	D35	140	D39
41	D16	42	D20	141	D40	142	D44
43	D17	44	D21	143	VDD	144	VDD
45	VDD	46	VDD	145	D41	146	D45
47	DQS2	48	DM2	147	DQS5	148	DM5
49	D18	50	D22	149	VSS	150	VSS
51	VSS	52	VSS	151	D42	152	D46
53	D19	54	D23	153	D43	154	D47
55	D24	56	D28	155	VDD	156	VDD
57	VDD	58	VDD	157	VDD	158	/CK1
59	D25	60	D29	159	VSS	160	CK1
61	DQS3	62	DM3	161	VSS	162	VSS
63	VSS	64	VSS	163	D48	164	D52
65	D26	66	D30	165	D49	166	D53
67	D27	68	D31	167	VDD	168	VDD
69	VDD	70	VDD	169	DQS6	170	DM6
71	CB0	72	CB4	171	D50	172	D54
73	CB1	74	CB5	173	VSS	174	VSS
75	VSS	76	VSS	175	D51	176	D55
77	DQS8	78	DM8	177	D56	178	D60
79	CB2	80	CB6	179	VDD	180	VDD
81	VDD	82	VDD	181	D57	182	D61
83	CB3	84	CB7	183	DQS7	184	DM7
85	NC	86	NC	185	VSS	186	VSS
87	VSS	88	VSS	187	D58	188	D62
89	CK2	90	VSS	189	D59	190	D63
91	/CK2	92	VDD	191	VDD	192	VDD
93	VDD	94	VDD	193	SDA	194	SA0
95	CKE1	96	CKE0	195	SCL	196	SA1
97	NC	98	NC	197	VDDSPD	198	SA2
99	A12	100	A11	199	VDDID	200	NC

Table 7 - Pin Description			
Pin Name	Description	Pin Name	Description
VDD	SDRAM positive power supply	VSS	Power supply return (ground)
VREF	Input or Output reference supply	VDDSPD	EEPROM power
VDDID	Voltage Identification Flag	/S0-/S1	Chip Select
A0-A12	Address Input	BA0-BA1	SDRAM Bank Address
CB0-CB7	Data check bit	DM0-DM8	Data Mask
DQS0-DQS8	Data Strobe	/WE	Write Enable
D0-D63	Data Bus	/CAS	Column address strobe
/RAS	Row address strobe	/CK0-/CK2	Clock Input (Negative)
CK0-CK2	Clock Input (Positive)	SCL	EEPROM Clock Input
CKE0-CKE1	Clock Enable	SDA	EEPROM Data Input or Output
SA0-SA2	EEPROM slave address select	NC	Spare Pin (no connect)

Figure 1 –Module Dimension 200 Pin DDR SDRAM Unbuffered SO-DIMM



Symbol	MIN	NOM	MAX
A	31.60	31.75	31.90
A1		6.00 BSC	
A4		20.00 BSC	
D	67.45	67.60	67.75
D2		63.60 BSC	
D3		1.80 BSC	
D4		1.50 BSC	
e1		11.40 BSC	
e2		47.40 BSC	
E			3.80

Notes:

1 All dimensioning and tolerance conform to ASME Y14.5M–1994.
2 Tolerance on all dimensions ± 0.15 unless otherwise specified.
3 All dimensions are in millimeters.