Datasheet | Rev. 2.0 | 2017

IMM1G72D3(L)SOD8AG (Die Revision A)
8GByte (1024M x 72 Bit)

8GB DDR3 ECC Unbuffered SO-DIMM
RoHS Compliant Product

Version: Rev. 2.0, Jan 2017

2.0 – Update the SPD information in Table 19

Version: Rev. 1.0, Aug 2014

1.0 – Initial release

Remark:
Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures .

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Features

- 204-Pin Unbuffered Small Outline Dual-In-Line Memory Module
- Capacity: 8GB
- JEDEC-Standard
- Bi-directional Differential Data-Strobe
- 72 Bit Data Bus Width with ECC
- Programmable CAS Latency (CL):
  - PC3-12800: 5, 6, 7, 8, 9, 10, 11
  - PC3-10600: 5, 6, 7, 8, 9, 10
- Programmable CAS Write Latency (CWL):
  - PC3-12800: 5, 6, 7, 8
  - PC3-10600: 5, 6, 7
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- On-Die Termination (ODT)
- ZQ Calibration Supported
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Asynchronous Reset
- On-board I2C Temperature Sensor with Integrated Serial Presence Detect (SPD) EEPROM
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 30.00mm (1.181 inch)

Table 1 - Ordering Information for RoHS Compliant Product				
Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM1G72D3xSOD8AG-Azzzy	8GB	1Gx72	2	8GB DDR3 ECC Unbuffed SO-DIMM

Notes:
x: Operating Voltage
y: Operating Temperature
zzz: Speed Grade

Table 2 - Operating Voltage	
Part Number	Operating Voltage
Blank	VDD, VDDQ = 1.5V (1.425V-1.575V)
L	VDD, VDDQ = 1.35V (1.283V-1.45V) Backward compatible to VDD, VDDQ = 1.5V (1.425V-1.575V)

Table 3 - Temperature Grade		
Part Number	Temperature Grade	T_{case}
Blank	Commercial temperature	0°C to 95°C
I	Industrial temperature	-40°C to 95°C

Remark: Tcase is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85 °C < Tcase <= 95 °C.

Table 4 - Speed Grade		
Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
125	PC3-12800 (DDR3-1600)	800MHz (1.25ns@CL=11)
15E	PC3-10600 (DDR3-1333)	667MHz (1.5ns@CL=9)

Table 5 - Memory Chip Information					
Part Number	Base Device Brand	Base device	Voltage	Type	Chip Packing
IMM1G72D3LSOD8AG-Azzzy	I'M	IM4G08D3FABG	1.35V	512Mx8	Lead Free
IMM1G72D3SOD8AG-Azzzy	I'M	IM4G08D3EABG	1.5V	512Mx8	Lead Free

Part Number Decoder

IMM 1G72 D3 (L) SO D 8 A G - A 125 (I)

Intelligent Memory Module

Module Configuration
1G72 = 1Gx72 (8GB)

Memory Type
D3 = DDR3

DDR3L option
Blank = 1.5 Volt
L = 1.35 or 1.5 Volt (DDR3L)

Module Form-Factor
SO = SO-DIMM

Number of Ranks
D = Dual Rank

DRAM Bit width
8 = using x8 components

Module PCB Revision
A = Revision A
B = Revision B
C = Revision C

RoHS compliance
G = Green / RoHS

IC Revision
A = Revision A
B = Revision B
C = Revision C

Speed Grade
15E = PC3-10600 / DDR3 1333
125 = PC3-12800 / DDR3 1600

Temperature Grade
Blank = Commercial Temperature (0°C to 95°C T_C)
I = Industrial Temperature (-40°C to 95°C T_C)

Table 6 - Addressing

Parameter	8GB
Refresh count	8K
Row address	64K A[15:0]
Device bank address	8 BA[2:0]
Device configuration	4Gb (512Mx8)
Column address	1K A[9:0]
Module rank address	2 /S[1:0]
Number of devices	18

Table 7 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	2	VSS	103	A3	104	A4
3	VSS	4	D4	105	A1	106	A2
5	D0	6	D5	107	A0	108	BA1
7	D1	8	VSS	109	VDD	110	VDD
9	VSS	10	/DQS0	111	CK0	112	CK1
11	DM0	12	DQS0	113	/CK0	114	/CK1
13	D2	14	VSS	115	VDD	116	VDD
15	D3	16	D6	117	A10/AP	118	NC
17	VSS	18	D7	119	BA0	120	NC
19	D8	20	VSS	121	/WE	122	/RAS
21	D9	22	D12	123	VDD	124	VDD
23	VSS	24	D13	125	/CAS	126	ODT0
25	/DQS1	26	VSS	127	/S0	128	ODT1
27	DQS1	28	DM1	129	/S1	130	A13
29	VSS	30	/RESET	131	VDD	132	VDD
31	D10	32	VSS	133	D32	134	D36
33	D11	34	D14	135	D33	136	D37
35	VSS	36	D15	137	VSS	138	VSS
37	D16	38	VSS	139	/DQS4	140	DM4
39	D17	40	D20	141	DQS4	142	D38
41	VSS	42	D21	143	VSS	144	D39
43	/DQS2	44	DM2	145	D34	146	VSS
45	DQS2	46	VSS	147	D35	148	D44
47	VSS	48	D22	149	VSS	150	D45
49	D18	50	D23	151	D40	152	VSS
51	D19	52	VSS	153	D41	154	/DQS5
53	VSS	54	D28	155	VSS	156	DQS5
55	D24	56	D29	157	DM5	158	VSS
57	D25	58	VSS	159	D42	160	D46
59	DM3	60	/DQS3	161	D43	162	D47
61	VSS	62	DQS3	163	VSS	164	VSS
63	D26	64	VSS	165	D48	166	D52
65	D27	66	D30	167	D49	168	D53
67	VSS	68	D31	169	VSS	170	VSS
69	CB0	70	VSS	171	/DQS6	172	DM6
71	CB1	72	CB4	173	DQS6	174	D54
73	VSS	74	CB5	175	VSS	176	D55
75	/DQS8	76	DM8	177	D50	178	VSS
77	DQS8	78	VSS	179	D51	180	D60
79	VSS	80	CB6	181	VSS	182	D61
81	CB2	82	CB7	183	D56	184	VSS
83	CB3	84	VREFCA	185	D57	186	/DQS7
85	VDD	86	VDD	187	VSS	188	DQS7
87	CKE0	88	A15	189	DM7	190	VSS
89	CKE1	90	A14	191	D58	192	D62
91	BA2	92	A9	193	D59	194	D63
93	VDD	94	VDD	195	VSS	196	VSS
95	A12, /BC	96	A11	197	SA0	198	/EVENT
97	A8	98	A7	199	VDDSPD	200	SDA
99	A5	100	A6	201	SA1	202	SCL
101	VDD	102	VDD	203	VTT	204	VTT

Table 8 - Pin Description			
Pin Name	Description	Pin Name	Description
VDD	SDRAM core power supply	VREFDQ	SDRAM I/O reference supply
VREFCA	SDRAM command/address reference supply	VSS	Power supply return (ground)
A0-A15	SDRAM address bus	BA0-BA2	SDRAM bank addresses
CK0-CK1	SDRAM clocks (positive line of differential pair)	/CK0-/CK1	SDRAM clocks (negative line of differential pair)
/RAS	SDRAM row address strobe	/CAS	SDRAM column address strobe
/WE	SDRAM write enable	CKE0-CKE1	SDRAM clock enable lines
/S0-/S1	DIMM Rank Select Lines	ODT0-ODT1	On-die termination control lines
DQS0-DQS8	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS8	SDRAM data strobes (negative line of differential pair)
D0-D63	DIMM memory data bus	DM0-DM8	SDRAM data mask/high data strobes
CB0-CB7	DIMM ECC Check bit	NC	Spare Pins (no connect)
SCL	EEPROM clock	SDA	EEPROM date line
SA0-SA1	EEPROM address input	VDDSPD	EEPROM positive power supply
/RESET	Reset Pin	VTT	Termination Voltage

Figure 1 – Module Dimension 204 Pin DDR3 SDRAM Unbuffered SO-DIMM

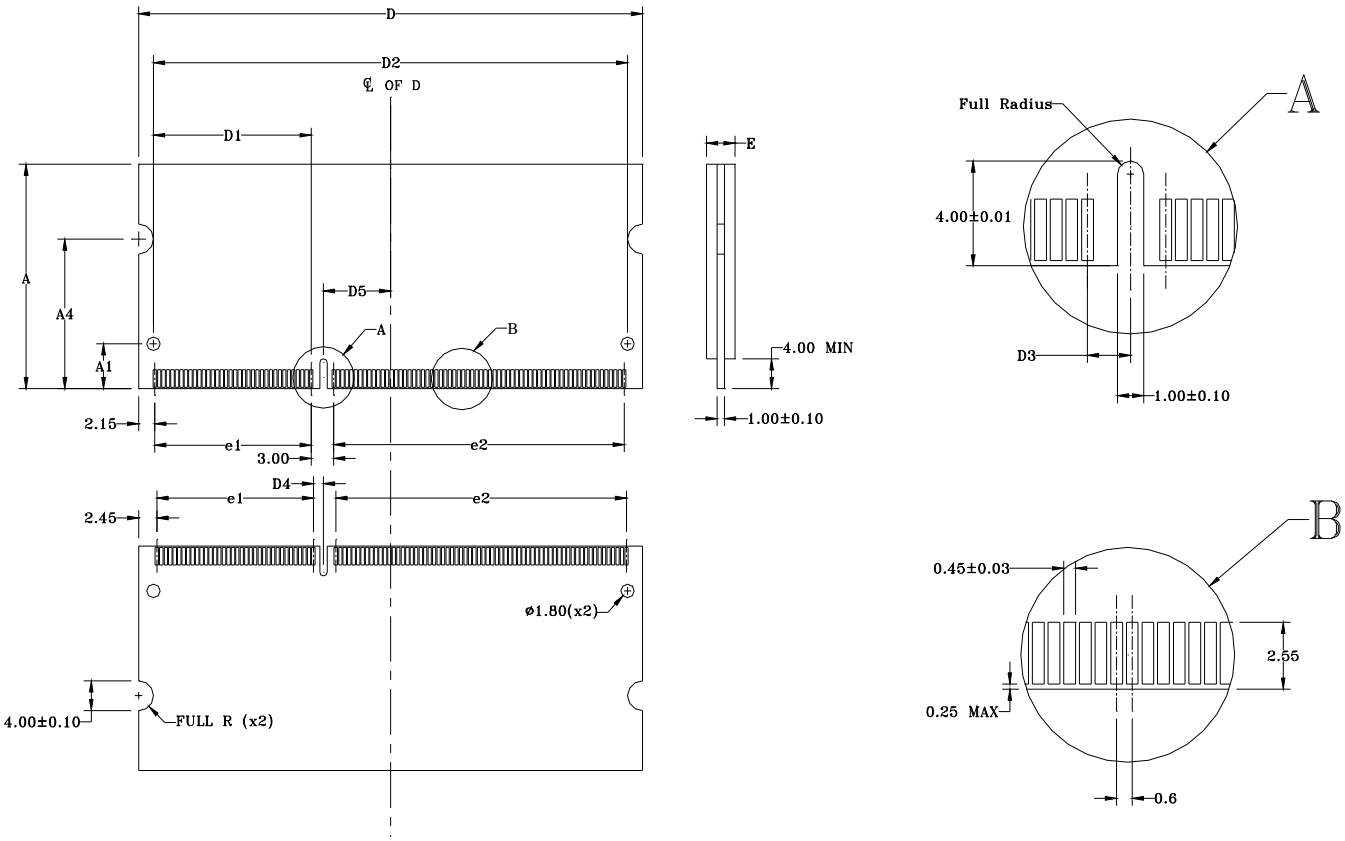


Table 9 - PCB Dimension			
Symbol	MIN	NOM	MAX
A	29.85	30.00	30.15
A1		20.00 Basic	
D	67.45	67.60	67.75
D2		63.60 Basic	
D3		1.65 Basic	
D5		9.00 Basic	
e1		21.00 Basic	
e2		39.00 Basic	
E			3.80

Notes:

- All dimensioning and tolerancing conform to ASME Y14.5M-1994.
- Tolerances for all dimensions ±0.15 unless otherwise specified.
- All dimensions are in millimeters.

Figure 2 – Functional Block Diagram (Page 1 of 2)

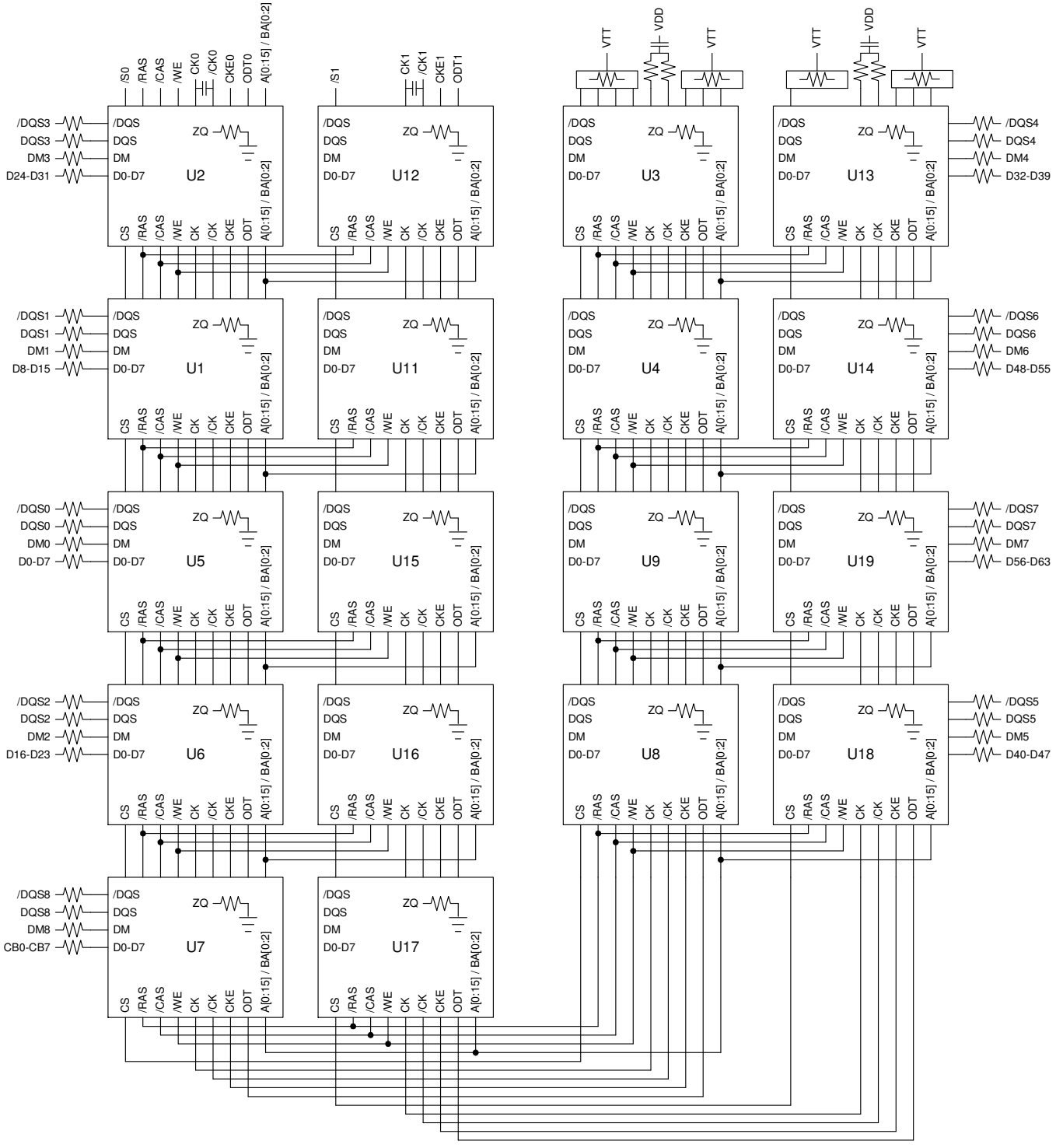
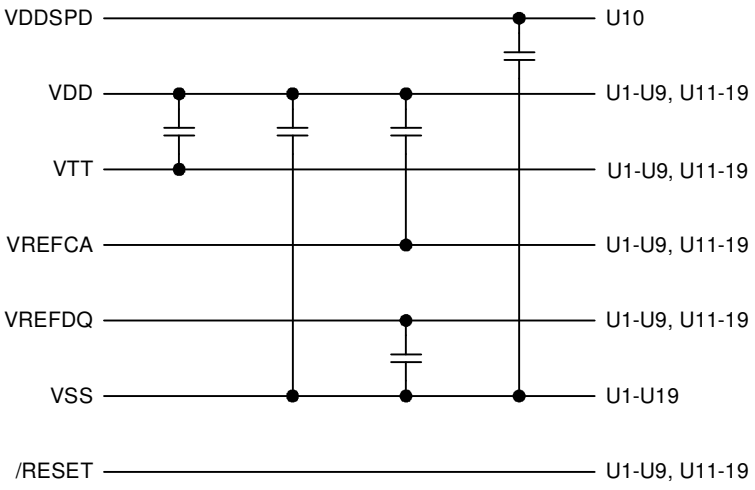
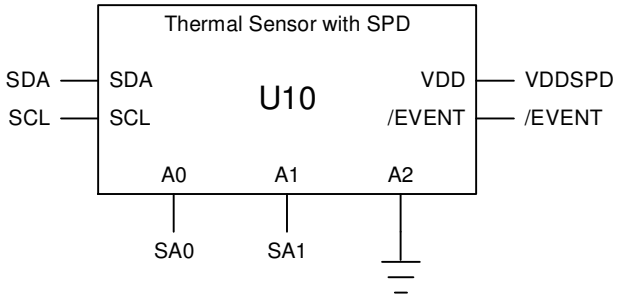


Figure 3 – Functional Block Diagram (Page 2 of 2)





Electrical Parameter

Table 10 - Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on V_{DD}, pin relative to V_{SS}	V_{DD}	-0.4V ~ 1.975	V	1,3
Voltage on V_{DDQ}, pin relative to V_{SS}	V_{DDQ}	-0.4V ~ 1.975	V	1,3
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	-0.4V ~ 1.975	V	1
DRAM Storage temperature	T_{STG}	-55 ~ 100	°C	1,2
DRAM Operation temperature	T_{case}	0 ~ 95	°C	2,4,5

Notes:

1 Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2 Storage Temperature or DRAM operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

3 VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6 x VDDQ, when VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

4 The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85 °C under all operating conditions.

5 Some applications require operation of the Extended Temperature Range between 85 °C and 95 °C case temperature. Full Specifications are guaranteed in this range but the following additional conditions apply a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us. b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

Table 11 - DC Electrical Characteristics and Operating Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ.	Max		
Supply voltage	V_{DD}	1.283	1.35	1.45	V	1,2
I/O supply voltage	V_{DDQ}				V	1,2
Supply voltage	V_{DD}	1.425	1.5	1.575	V	1,2,3
I/O supply voltage	V_{DDQ}				V	1,2,3

Notes:

1. VDD and VDDQ must track one another. VDDQ must be less than or equal to VDD. VSS = VSSQ.
2. VDD and VDDQ may include AC noise of +/-50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. VDD and VDDQ must be at same level for valid AC timing parameters.
3. Module is backward-compatible with 1.5V operation.

Table 12 - DC Electrical Characteristics and Input Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ.	Max		
V_{IN} low; DC/commands/address buses (1.35V Operation)	V_{IL}	V_{SS}	-	-0.090	V	
V_{IN} low; DC/commands/address buses (1.5V Operation)	V_{IL}	V_{SS}	-	-0.100	V	
V_{IN} high; DC/commands/address buses (1.35V Operation)	V_{IH}	0.090	-	V_{DD}	V	
V_{IN} high; DC/commands/address buses (1.5V Operation)	V_{IH}	0.100	-	V_{DD}	V	
Input reference voltage; command/address bus	$V_{REFCA(DC)}$	0.49* V_{DD}	0.50* V_{DD}	0.51* V_{DD}	V	1,2
I/O reference voltage DQ bus	$V_{REFDQ(DC)}$	0.49* V_{DD}	0.50* V_{DD}	0.51* V_{DD}	V	2,3
Command/address termination voltage (system level, not direct DRAM input)	V_{TT}	-	0.50* V_{DDq}	-	V	4

Notes:

1. VREFCA(DC) is expected to be approximately 0.5 × VDD and to track variations in the DC level. Externally generated peak noise (noncommon mode) on VREFCA may not exceed ±1% × VDD around the VREFCA(DC) value. Peak-to-peak AC noise on VREFCA should not exceed ±2% of VREFCA(DC).
2. DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20 MHz in frequency.
3. VREFDQ(DC) is expected to be approximately 0.5 × VDD and to track variations in the DC level. Externally generated peak noise (noncommon mode) on VREFDQ may not exceed ±1% × VDD around the VREFDQ(DC) value. Peak-to-peak AC noise on VREFDQ should not exceed ±2% of VREFDQ(DC).
4. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors. MIN and MAX values are system-dependent.

Table 13 - Input Switching Conditions				
Parameter / Condition	Symbol	Value		Units
		1.35V Operation	1.5V Operation	
Command and Address				
Input high AC voltage: Logic 1 @ 175mV	$V_{IH(AC175)min}$	-	175	mV
Input high AC voltage: Logic 1 @ 160mV	$V_{IH(AC160)min}$	160	-	mV
Input high AC voltage: Logic 1 @ 150mV	$V_{IH(AC150)min}$	-	150	mV
Input high AC voltage: Logic 1 @ 135mV	$V_{IH(AC135)min}$	135	-	mV
Input high DC voltage: Logic 1 @ 100mV	$V_{IH(DC100)min}$	-	100	mV
Input high DC voltage: Logic 1 @ 90mV	$V_{IH(DC90)min}$	90	-	mV
Input low DC voltage: Logic 0 @ -90mV	$V_{IL(DC90)max}$	-90	-	mV
Input low DC voltage: Logic 0 @ -100mV	$V_{IL(DC100)max}$	-	-100	mV
Input low AC voltage: Logic 0 @ -135mV	$V_{IL(AC135)max}$	-135	-	mV
Input low AC voltage: Logic 0 @ -150mV	$V_{IL(AC150)max}$	-	-150	mV
Input low AC voltage: Logic 0 @ -160mV	$V_{IL(AC160)max}$	-160	-	mV
Input low AC voltage: Logic 0 @ -175mV	$V_{IL(AC175)max}$	-	-175	mV
DQ and DM				
Input high AC voltage: Logic 1	$V_{IH(AC160)min}$	160	-	mV
Input high AC voltage: Logic 1	$V_{IH(AC150)min}$	-	150	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}$	135	135	mV
Input high DC voltage: Logic 1	$V_{IH(DC100)min}$	-	100	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	-	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)max}$	-90	-	mV
Input low DC voltage: Logic 0	$V_{IL(DC100)max}$	-	-100	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)max}$	-135	-135	mV
Input low AC voltage: Logic 0	$V_{IL(AC150)max}$	-	-150	mV
Input low AC voltage: Logic 0	$V_{IL(AC160)max}$	-160	-	mV

Notes:

1. All voltages are referenced to VREF. VREF is VREFCA for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. VREF is VREFDQ for DQ and DM inputs.
2. Input setup timing parameters (tIS and tDS) are referenced at VIL(AC)/VIH(AC), not VREF(DC).
3. Input hold timing parameters (tIH and tDH) are referenced at VIL(DC)/VIH(DC), not VREF(DC).
4. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).

Table 14 - Differential Input Operating Conditions (CK, /CK and DQS, /DQS)					
Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Differential input voltage logic high - slew (1.35V Operation)	$V_{IH,diff}$	+180	-	mV	1
Differential input voltage logic high - slew (1.5V Operation)	$V_{IH,diff}$	+200	-	mV	1
Differential input voltage logic low - slew (1.35V Operation)	$V_{IL,diff}$	-	-180	mV	1
Differential input voltage logic low - slew (1.5V Operation)	$V_{IL,diff}$	-	-200	mV	1
Differential input voltage logic high	$V_{IH,diff(AC)}$	2* ($V_{IH(AC)}$ - V_{REF})	-	mV	2
Differential input voltage logic low	$V_{IL,diff(AC)}$	-	2* ($V_{IL(AC)}$ - V_{REF})	mV	3
Single-ended high level for strobes (1.35V Operation)	V_{SEH}	V_{DDQ}/2 + 175	-	mV	2
Single-ended high level for CK, /CK (1.35V Operation)		V_{DD}/2 + 175	-	mV	2
Single-ended high level for strobes (1.5V Operation)	V_{SEH}	V_{DDQ}/2 + 175	-	mV	2
Single-ended high level for CK, /CK (1.5V Operation)		V_{DD}/2 + 175	-	mV	2
Single-ended low level for strobes (1.35V Operation)	V_{SEL}	-	V_{DDQ}/2 - 175	mV	3
Single-ended low level for CK, /CK (1.35V Operation)		-	V_{DD}/2 – 175	mV	3
Single-ended low level for strobes (1.5V Operation)	V_{SEL}	-	V_{DDQ}/2 - 175	mV	3
Single-ended low level for CK, /CK (1.5V Operation)		-	V_{DD}/2 - 175	mV	3

Notes:

1. Defines slew rate reference points, relative to input crossing voltages.
2. Minimum DC limit is relative to single-ended signals; overshoot specifications are applicable.
3. Maximum DC limit is relative to single-ended signals; undershoot specifications are applicable.

Table 15 - Single-Ended Output Driver Characteristics					
Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{TT} - 0.1 * V_{DDQ}$ and $V_{OH(AC)} = V_{TT} + 0.1 * V_{DDQ}$ (1.35V Operation)	SRQ_{se}	1.75	5	V/ns	1,2,3
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{TT} - 0.1 * V_{DDQ}$ and $V_{OH(AC)} = V_{TT} + 0.1 * V_{DDQ}$ (1.5V Operation)	SRQ_{se}	2.5	5	V/ns	1,2,3
Single-ended DC high-level output voltage	$V_{OH(DC)}$	$0.8 * V_{DDQ}$		V	1,2
Single-ended DC mid-level output voltage	$V_{OM(DC)}$	$0.5 * V_{DDQ}$		V	1,2
Single-ended DC low-level output voltage	$V_{OL(DC)}$	$0.2 * V_{DDQ}$		V	1,2
Single-ended AC high-level output voltage	$V_{OH(AC)}$	$V_{TT} + 0.1 * V_{DDQ}$		V	1,2
Single-ended AC low-level output voltage	$V_{OL(AC)}$	$V_{TT} - 0.1 * V_{DDQ}$		V	1,2
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				

Notes:

1. RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (VDDQ = VDD, VSSQ = VSS).
2. VTT = VDDQ/2.
3. The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or all switching the opposite direction. For all other DQ signal switching combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.

Table 16 - Differential Output Driver Characteristics					
Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)}$, = -0.2 * V_{DDQ} and $V_{OH,diff(AC)}$ = + 0.2 * V_{DDQ} (1.35V Operation)	SRQ_{diff}	3.5	12	V/ns	1
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)}$, = -0.2 * V_{DDQ} and $V_{OH,diff(AC)}$ = + 0.2 * V_{DDQ} (1.5V Operation)	SRQ_{diff}	5	10	V/ns	1
Differential high-level output voltage	$V_{OH,diff(AC)}$	+0.2 * V_{DDQ}		V	1
Differential low-level output voltage	$V_{OL,diff(AC)}$	-0.2 * V_{DDQ}		V	1
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				

Notes:

1. RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (VDDQ = VDD, VSSQ = VSS).
2. VREF = VDDQ/2; slew rate @ 5V/ns, interpolate for faster slew rate.

For part number IMM1G72D3(L)SOD8AG-A125(I)

Table 17 - IDD Specifications with Conditions and Operation Current

Parameter / Condition	Symbol	Current		Units	Notes
		1.35V Operation	1.5V Operation		
Operating current 0; One bank ACTIVATE-to-PRECHARGE	I_{DD0}	495	495	mA	1, 2
Operating current 1; One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	630	630	mA	1, 2
Precharge power-down current; Slow exit	I_{DD2P0}	180	180	mA	1, 2
Precharge power-down current; Fast exit	I_{DD2P1}	288	288	mA	1, 2
Precharge quiet standby current	I_{DD2Q}	450	450	mA	1, 2
Precharge standby current	I_{DD2N}	360	360	mA	1, 2
Precharge standby ODT current	I_{DD2NT}	540	540	mA	1, 2
Active power-down current	I_{DD3P}	270	270	mA	1, 2
Active standby current	I_{DD3N}	540	540	mA	1, 2
Burst read operating current	I_{DD4R}	855	855	mA	1, 2
Burst write operating current	I_{DD4W}	900	900	mA	1, 2
Refresh current	I_{DD5B}	1530	1530	mA	1, 2
Self refresh temperature current: MAX T_c = 85°C	I_{DD6}	180	180	mA	1, 2
Self refresh temperature current (SRT-enabled): MAX T_c = 95°C	I_{DD6ET}	270	270	mA	1, 2
All banks interleaved read current	I_{DD7}	1440	1440	mA	1, 2
Reset current	I_{DD8}	180	180	mA	1, 2

Notes:

1 Value shown for DDR3 SDRAM only and are computed from values specified in the 4Gbit component data sheet.

2 One module rank in the active IDD, the other rank in IDD2P0.

3 All ranks in this IDD conditions.

For part number IMM1G72D3(L)SOD8AG-A125(I)

Table 18 - AC Timing Parameter and Operating Conditions

Parameter / Condition		Symbol	Min	Max	Units
Clock Timing					
Clock period average: DLL disable mode	T_C = 0°C to 85°C	tCK (DLL_DIS)	8	7800	ns
	T_C => 85°C to 95°C		8	3900	
Clock periods average: DLL enable mode (CL = 11, CWL = 8)		tCK (AVG)	1.25	<1.5	ns
Clock periods average: DLL enable mode (CL = 9, CWL = 7)		tCK (AVG)	1.5	<1.875	ns
High pulse width average		tCH (AVG)	0.47	0.53	tCK
Low pulse width average		tCL (AVG)	0.47	0.53	tCK
Clock period jitter	DLL locked	tJITper	-70	70	ps
	DLL locking	tJITper,lck	-60	60	ps
Clock absolute period		tCK (ABS)	tCK (AVG) MIN + tJITper MIN	tCK (AVG) MAX + tJITper MAX	ps
Clock absolute high pulse width		tCH (ABS)	0.43	-	tCK (AVG)
Clock absolute low pulse width		tCL (ABS)	0.43	-	tCK (AVG)
Cycle-to-cycle jitter	DLL locked	tJITcc	140		ps
	DLL locking	tJITcc,lck	120		ps
Cumulative error across	2 cycles	tERR2per	-103	103	ps
	3 cycles	tERR3per	-122	122	ps
	4 cycles	tERR4per	-136	136	ps
	5 cycles	tERR5per	-147	147	ps
	6 cycles	tERR6per	-155	155	ps
	7 cycles	tERR7per	-163	163	ps
	8 cycles	tERR8per	-169	169	ps
	9 cycles	tERR9per	-175	175	ps
	10 cycles	tERR10per	-180	180	ps
	11 cycles	tERR11per	-184	184	ps
	12 cycles	tERR12per	-188	188	ps
	n = 14,…49, 50 cycles	tERRnper	(1+0.68ln[n]) * tJITper MIN	(1+0.68ln[n]) * tJITper Max	ps
DQ Input Timing					
Data setup time to DQS, /DQS (1.35V Operation)	Base (specification)	tDS (AC135)	25	-	ps
					ps
Data setup time to DQS, /DQS (1.5V Operation)	Base (specification)	tDS (AC150)	10	-	ps
					ps
Data hold time from DQS, /DQS (1.35V Operation)	Base (specification)	tDH (DC90)	55	-	ps
					ps
Data hold time from DQS, /DQS (1.5V Operation)	Base (specification)	tDH (DC100)	45	-	ps
					ps
Minimum data pulse width		tDIPW	360	-	ps
DQ Output Timing					
DQS, /DQS to DQ skew, per access		tDQSQ	-	100	ps
DQ output hold time from DQS, /DQS		tQH	0.38	-	tCK (AVG)
DQ Low-Z time from CK, /CK		tLZDQ	-450	225	ps
DQ High-Z time from CK, /CK		tHZDQ	-	225	ps
DQ Strobe Input Timing					
DQS, /DQS rising to CK, /CK rising		tDQSS	-0.27	0.27	tCK
DQS, /DQS differential input low pulse width		tDQSL	0.45	0.55	tCK

For part number IMM1G72D3(L)SOD8AG-A125(I)

Parameter / Condition		Symbol	Min	Max	Units
DQS, /DQS falling setup to CK, /CK rising		tDSS	0.18	-	tCK
DQS, /DQS falling hold from CK, /CK rising		tDSH	0.18	-	tCK
DQS, /DQS differential input high pulse width		tDQSH	0.45	0.55	tCK
DQS, /DQS differential WRITE preamble		tWPRE	0.9	-	tCK
DQS, /DQS differential WRITE postamble		tWPST	0.3	-	tCK
DQ Strobe Output Timing					
DQS, /DQS rising to/from CK, /CK		tDQSCK	-225	225	ps
DQS, /DQS differential output high time		tQSH	0.40	-	tCK
DQS, /DQS differential output low time		tQSL	0.40	-	tCK
DQS, /DQS Low-Z time (RL-1)		tLZDQS	-450	225	ps
DQS, /DQS High-Z time (RL+BL/2)		tHZDQS	-	225	ps
DQS, /DQS differential READ preamble		tRPRE	0.9	greater of tLZ(DQS) (MAX), tDQSK (MAX)	tCK
DQS, /DQS differential READ postamble		tRPST	0.3	greater of tDQSCK (MIN) + tQSH (MIN), tHZ(DQS) (MAX)	tCK
Command and Address Timing					
DLL locking time		tDLLK	512	-	tCK
CTRL, CMD, ADDR setup to CK, /CK (1.35V Operation)	Base (specification)	tIS (AC160)	60	-	ps ps
CTRL, CMD, ADDR setup to CK, /CK (1.35V Operation)	Base (specification)	tIS (AC135)	185	-	ps ps
CTRL, CMD, ADDR setup to CK, /CK (1.5V Operation)	Base (specification)	tIS (AC175)	45	- -	ps ps
CTRL, CMD, ADDR setup to CK, /CK (1.5V Operation)	Base (specification)	tIS (AC150)	170	-	ps ps
CTRL, CMD, ADDR hold from CK, /CK (1.35V Operation)	Base (specification)	tIH (DC90)	130	-	ps ps
CTRL, CMD, ADDR hold from CK, /CK (1.5V Operation)	Base (specification)	tIH (DC100)	120	-	ps ps
Minimum CTRL, CMD, ADDR pulse width		tIPW	560	-	ps
ACTIVATE to internal READ or WRITE delay		tRCD	13.125	-	ns
PRECHARGE command period		tRP	13.125	-	ns
ACTIVATE-to-PRECHARGE command period		tRAS	35	9 * tREFI	ns
ACTIVATE-to-ACTIVATE command period		tRC	48.125	-	ns
ACTIVATE-to-ACTIVATE minimum period		tRRD	greater of 4tCK or 7.5ns	-	tCK
Four ACTIVATE windows (2KB page size)		tFAW	40	-	ns
Write recovery time		tWR	15	-	ns
Delay from start of internal WRITE transaction to internal READ command		tWTR	greater of 4tCK or 7.5ns	-	tCK
READ-to-PRECHARGE time		tRTP	greater of 4tCK or 7.5ns	-	tCK
/CAS-to-/CAS command delay		tCCD	4tCK	-	tCK
Auto precharge write recovery + precharge time		tDAL	WR + tRP/ tCK (AVG)	-	tCK
MODE REGISTER SET command cycle time		tMRD	4tCK	-	tCK
MODE REGISTER SET command update delay		tMOD	greater of 12tCK or 15ns	-	tCK
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		tMPRR	1tCK	-	tCK

For part number IMM1G72D3(L)SOD8AG-A125(I)

Parameter / Condition		Symbol	Min	Max	Units
Calibration Timing					
ZQCL command: Long calibration time	POWER-UP and RESET operation	tZQinit	greater of 512 tCK	-	tCK
	Normal operation	tZQoper	greater of 256 tCK	-	tCK
ZQCS command: Short calibration time		tZQcs	greater of 64 tCK	-	tCK
Initialization and Reset Timing					
Exit reset from CKE HIGH to valid command		tXPR	greater of 5tCK or tRFC(min)+10ns	-	tCK
Refresh Timing					
REFRESH-to-ACTIVATE or REFRESH command period		tRFC	260	-	ns
Maximum refresh period	T_c<=85°C	-	64 (1X)		ms
	T_c>85°C		32 (2X)		
Maximum average periodic refresh	T_c<=85°C	tREFI	7.8 (64ms/8192)		us
	T_c>85°C		3.9 (32ms/8192)		
Self Refresh Timing					
Exit self refresh to commands not requiring a locked DLL		tXS	greater of 5 tCK or tRFC+10ns	-	tCK
Exit self refresh to commands requiring a locked DLL		tXSDLL	tDLLK (MIN)	-	tCK
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		tCKESR	tCKE (MIN) + tCK	-	tCK
Valid clocks after self refresh entry or power down entry		tCKSRE	greater of 5tCK or 10ns	-	tCK
Valid clocks before self refresh exit, power-down exit, or reset exit		tCKSRX	greater of 5tCK or 10ns	-	tCK
Power-Down Timing					
CKE MIN pulse width		tCKE (MIN)	greater of 3tCK or 5ns		tCK
Command pass disable delay		tCPDED	2	-	tCK
Power-down entry to power exit timing		tPD	tCKE (MIN)	9 * tREFI	tCK
Power-Down Entry Minimum Timing					
ACTIVATE command to power-down entry		tACTPDEN	MIN = 1		tCK
PRECHARGE/PRECHARGE ALL command to power-down entry		tPRPDEN	MIN = 1		tCK
REFRESH command to power-down entry		tREFPDEN	MIN = 1		tCK
MRS command to power-down entry		tMRSPDEN	MIN = tMOD (MIN)		tCK
READ/READ with auto precharge command to power-down entry		tRDPDEN	MIN = RL + 4 + 1		tCK
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	tWRPDEN	MIN = WL + 4 + tWR/tCK (AVG)		tCK
	BC4MRS	tWRPDEN	MIN = WL + 2 + tWR/tCK (AVG)		tCK
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	tWRAPDEN	MIN = WL + 4 + tWR + 1		tCK
	BC4MRS	tWRAPDEN	MIN = WL + 2 + tWR + 1		tCK
Power-Down Exit Timing					
DLL on, any valid command, or DLL off to commands not requiring locked DLL		tXP	greater of 3tCK or 6ns	-	tCK
Precharge power-down with DLL off to commands requiring a locked DLL		tXPDLL	greater of 10tCK or 24ns	--	tCK

For part number IMM1G72D3(L)SOD8AG-A125(I)

Parameter / Condition	Symbol	Min	Max	Units
ODT Timing				
R_{TT} turn-on from ODTL on reference	^{t}AON	-225	225	ps
R_{TT} turn-off from ODTL off reference	^{t}AOF	0.3	0.7	CK
Asynchronous R_{TT} turn-on delay (power-down with DLL off)	^{t}AONPD	2	8.5	ns
Asynchronous R_{TT} turn-off delay (power-down with DLL off)	^{t}AOFPD	2	8.5	ns
ODT HIGH time with WRITE command and BL8	ODTH8	6	-	^{t}CK
ODT HIGH time without WRITE command or WRITE command and BC4	ODTH4	4	-	^{t}CK
Dynamic ODT Timing				
R_{TT} dynamic change skew	^{t}ADC	0.3	0.7	^{t}CK
Write Leveling Timing				
First DQS, /DQS rising edge	^{t}WLMRD	40	-	^{t}CK
DQS, /DQS delay	^{t}WLDQSEN	25	-	^{t}CK
Write leveling setup from rising CK, /CK crossing to rising DQS, /DQS crossing	^{t}WLS	165	-	ps
Write leveling hold from rising DQS, /DQS crossing to rising CK, /CK crossing	^{t}WLH	165	-	ps
Write leveling output delay	^{t}WLO	0	7.5	ns
Write leveling output error	^{t}WLOE	0	2	ns

For part number IMM1G72D3(L)SOD8AG-A125(I)

Table 19 - SPD Information

Byte NO.	Description	Note		Hex	
		1.35V Operation	1.5V Operation	1.35V Operation	1.5V Operation
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	176 / 256 / 0-116		92	
1	SPD Revision	1.2		12	
2	Key Byte / DRAM Device Type	DDR3 SDRAM		0B	
3	Key Byte / Module Type	72b Unbuffered SO-DIMM		08	
4	SDRAM Density and Banks	4Gb 8banks		04	
5	SDRAM Addressing	Row 16 / Col 10		21	
6	Module Nominal Voltage, VDD	1.35V/1.5V	1.5V	02	00
7	Module Organization	2Rank , x8		09	
8	Module Memory Bus Width	ECC, 72bit		0B	
9	Fine Timebase (FTB) Dividend and Divisor	2.5ps		52	
10	Medium Timebase (MTB) Dividend	1/8 (0.125ns)		01	
11	Medium Timebase (MTB) Divisor	1/8 (0.125ns)		08	
12	SDRAM Minimum Cycle Time (tCKmin)	1.25ns		0A	
13	Reserved	-		00	
14	CAS Latencies Supported, Least Significant Byte	5, 6, 7, 8, 9, 10, 11		FE	
15	CAS Latencies Supported, Most Significant Byte	-		00	
16	Minimum CAS Latency Time (tAAmin)	13.125ns		69	
17	Minimum Write Recovery Time (tWRmin)	15ns		78	
18	Minimum /RAS to /CAS Delay Time (tRCDmin)	13.125ns		69	
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	6.0ns		30	
20	Minimum Row Precharge Time (tRPmin)	13.125ns		69	
21	Upper Nibbles for tRAS and tRC	-		11	
22	Minimum Active to Precharge Time (tRASmin), LSB	35ns		18	
23	Minimum Active to Active/Refresh Time (tRCmin), LSB	48.125ns		81	
24	Minimum Refresh Recovery Time (tRFCmin), LSB	260ns		20	
25	Minimum Refresh Recovery Time (tRFCmin), MSB	260ns		08	
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	7.5ns		3C	
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns		3C	
28	Upper Nibble for tFAW	30ns		00	
29	Minimum Four Activate Window Delay Time (tFAWmin), LSB	30ns		F0	
30	SDRAM Optional Features	DLL off Mode, RZQ/6, RZQ/7		83	
31	SDRAM Thermal and Refresh Options	0-95oC Op. Temp. w/2x refresh		05	
32	Module Thermal Sensor	With TS		80	
33	SDRAM Device Type	Standard SDRAM		00	
34-59	Reserved, General Section	-		00	
60	Module Nominal Height	29< Height <= 30		0F	

Byte NO.	Description	Note		Hex	
		1.35V Operation	1.5V Operation	1.35V Operation	1.5V Operation
61	Module Maximum Thickness	1< Tf <=2 (mm); 1< Tb <=2 (mm)		11	
62	Reference Raw Card Used	JEDEC Raw Card D1		23	
63	Address Mapping from Edge Connector to DRAM	Non-Mirrored		00	
64-116	Module Type Specific Section, Indexed by Key Byte	-		00	
117-118	Module ID: Module Manufacturer's JEDEC ID Code	Reserved		Reserved	
119	Module ID: Module Manufacturing Location	Reserved		Reserved	
120-121	Module ID: Module Manufacturing Date	Reserved		Reserved	
122-125	Module ID: Module Serial Number	Reserved		Reserved	
126-127	Cyclical Redundancy Code	-		7C 59	D7 DE
128-145	Module Part Number	Reserved		Reserved	
146-147	Module Revision Code	Reserved		Reserved	
148-149	DRAM Manufacturer's JEDEC ID Code	Reserved		Reserved	
150-175	Manufacturer's Specific Data	Reserved		Reserved	
176-255	Open For Customer Use	Reserved		Reserved	

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