Datasheet | Rev. 1.0 | 2018

IMM2G64D3LSOD8AG (Die Revision C)
16GByte (2048M x 64 Bit)

16GB DDR3 Unbuffered SO-DIMM
RoHS Compliant Product

Remark:
Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures.

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Features

- 204-Pin Unbuffered Small Outline Dual-In-Line Memory Module
- Capacity: 16GB
- JEDEC-Standard
- Bi-directional Differential Data-Strobe
- 64 Bit Data Bus Width without ECC
- Programmable CAS Latency (CL):
  - PC3-12800: 5, 6, 7, 8, 9, 10, 11
  - PC3-10600: 5, 6, 7, 8, 9
- Programmable CAS Write Latency (CWL):
  - PC3-12800: 5, 6, 7, 8
  - PC3-10600: 5, 6, 7
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- On-Die Termination (ODT)
- ZQ Calibration Supported
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Asynchronous Reset
- Serial Presence Detect (SPD) EEPROM
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 30.00mm (1.181 inch)

Table 1 - Ordering Information for RoHS Compliant Product				
Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM2G64D3xSOD8AG-Czzzy	16GB	2Gx64	2	16GB DDR3 Unbuffed SO-DIMM

Notes:
- x: Operating Voltage
- y: Operating Temperature
- zzz: Speed Grade

Table 2 - Operating Voltage	
Part Number	Operating Voltage
L	V_{DD}, V_{DDQ} = 1.35V (1.283V-1.45V) Backward compatible to V_{DD}, V_{DDQ} = 1.5V (1.425V-1.575V)

Table 3 - Temperature Grade		
Part Number	Temperature Grade	T_{case}
Blank	Commercial temperature	0°C to 95°C
I	Industrial temperature	-40°C to 95°C

Remark: Tcase is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85 °C < T_{case} <= 95 °C.

Table 4 - Speed Grade		
Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
125	PC3-12800 (DDR3-1600)	800MHz (1.25ns@CL=11)
15E	PC3-10600 (DDR3-1333)	667MHz (1.5ns@CL=9)

Table 5 - Memory Chip Information					
Part Number	Base Device Brand	Base device	Voltage	Type	Chip Packing
IMM2G64D3LSOD8AG-Czzzy	I'M	IM8G08D3FCBG	1.35V	1024Mx8	Lead Free

Part Number Decoder

IMM 2G64 D3 L SO D 8 A G - C 125 (I)

Intelligent Memory Module

Module Configuration
2G64 = 2Gx64 (16GB)

Memory Type
D3 = DDR3

DDR3L option
L = 1.35 or 1.5 Volt (DDR3L)

Module Form-Factor
SO = Unbuffered SO-DIMM

Number of Ranks
D = Dual Rank

DRAM Bit width
8 = using x8 components

Module PCB Revision
A = Revision A

RoHS compliance
G = Green / RoHS

IC Revision
C = Revision C

Speed Grade
15E = PC3-10600 / DDR3 1333
125 = PC3-12800 / DDR3 1600

Temperature Grade
Blank = Commercial Temperature (0°C to 95°C T_C)
I = Industrial Temperature (-40°C to 95°C T_C)

Table 6 - Addressing

Parameter	16GB
Refresh count	8K
Row address	64K A[15:0]
Device bank address	8 BA[2:0]
Device configuration	8Gb (1024Mx8)
Column address	2K A[9:0], A11
Module rank address	2 /S[1:0]
Number of devices	16

Table 7 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{REFDQ}	2	V_{SS}	103	/CK0	104	/CK1
3	V_{SS}	4	D4	105	V_{DD}	106	V_{DD}
5	D0	6	D5	107	A10, AP	108	BA1
7	D1	8	V_{SS}	109	BA0	110	/RAS
9	V_{SS}	10	/DQS0	111	V_{DD}	112	V_{DD}
11	DM0	12	DQS0	113	/WE	114	/S0
13	V_{SS}	14	V_{SS}	115	/CAS	116	ODT0
15	D2	16	D6	117	V_{DD}	118	V_{DD}
17	D3	18	D7	119	A13	120	ODT1
19	V_{SS}	20	V_{SS}	121	/S1	122	NC
21	D8	22	D12	123	V_{DD}	124	V_{DD}
23	D9	24	D13	125	NC	126	V_{REFCA}
25	V_{SS}	26	V_{SS}	127	V_{SS}	128	V_{SS}
27	/DQS1	28	DM1	129	D32	130	D36
29	DQS1	30	/RESET	131	D33	132	D37
31	V_{SS}	32	V_{SS}	133	V_{SS}	134	V_{SS}
33	D10	34	D14	135	/DQS4	136	DM4
35	D11	36	D15	137	DQS4	138	V_{SS}
37	V_{SS}	38	V_{SS}	139	V_{SS}	140	D38
39	D16	40	D20	141	D34	142	D39
41	D17	42	D21	143	D35	144	V_{SS}
43	V_{SS}	44	V_{SS}	145	V_{SS}	146	D44
45	/DQS2	46	DM2	147	D40	148	D45
47	DQS2	48	V_{SS}	149	D41	150	V_{SS}
49	V_{SS}	50	D22	151	V_{SS}	152	/DQS5
51	D18	52	D23	153	DM5	154	DQS5
53	D19	54	V_{SS}	155	V_{SS}	156	V_{SS}
55	V_{SS}	56	D28	157	D42	158	D46
57	D24	58	D29	159	D43	160	D47
59	D25	60	V_{SS}	161	V_{SS}	162	V_{SS}
61	V_{SS}	62	/DQS3	163	D48	164	D52
63	DM3	64	DQS3	165	D49	166	D53
65	V_{SS}	66	V_{SS}	167	V_{SS}	168	V_{SS}
67	D26	68	D30	169	/DQS6	170	DM6
69	D27	70	D31	171	DQS6	172	V_{SS}
71	V_{SS}	72	V_{SS}	173	V_{SS}	174	D54
73	CKE0	74	CKE1	175	D50	176	D55
75	V_{DD}	76	V_{DD}	177	D51	178	V_{SS}
77	NC	78	A15	179	V_{SS}	180	D60
79	BA2	80	A14	181	D56	182	D61
81	V_{DD}	82	V_{DD}	183	D57	184	V_{SS}
83	A12,/BC	84	A11	185	V_{SS}	186	/DQS7
85	A9	86	A7	187	DM7	188	DQS7
87	V_{DD}	88	V_{DD}	189	V_{SS}	190	V_{SS}
89	A8	90	A6	191	D58	192	D62
91	A5	92	A4	193	D59	194	D63
93	V_{DD}	94	V_{DD}	195	V_{SS}	196	V_{SS}
95	A3	96	A2	197	SA0	198	NC
97	A1	98	A0	199	V_{DDSPD}	200	SDA
99	V_{DD}	100	V_{DD}	201	SA1	202	SCL
101	CK0	102	CK1	203	V_{TT}	204	V_{TT}

Table 8 - Pin Description			
Pin Name	Description	Pin Name	Description
V_{DD}	SDRAM core power supply	V_{REFDQ}	SDRAM I/O reference supply
V_{REFCA}	SDRAM command/address reference supply	V_{SS}	Power supply return (ground)
A0-A15	SDRAM address bus	BA0-BA2	SDRAM bank addresses
CK0-CK1	SDRAM clocks (positive line of differential pair)	/CK0-/CK1	SDRAM clocks (negative line of differential pair)
/RAS	SDRAM row address strobe	/CAS	SDRAM column address strobe
/WE	SDRAM write enable	CKE0-CKE1	SDRAM clock enable lines
/S0-/S1	DIMM Rank Select Lines	ODT0-ODT1	On-die termination control lines
DQS0-DQS7	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS7	SDRAM data strobes (negative line of differential pair)
D0-D63	DIMM memory data bus	DM0-DM7	SDRAM data mask/high data strobes
SCL	EEPROM clock	SDA	EEPROM date line
SA0-SA1	EEPROM address input	V_{DDSPD}	EEPROM positive power supply
/RESET	Reset Pin	V_{TT}	Termination Voltage
NC	Spare Pins (no connect)	-	-

Module Dimension

Figure 1 – 204 Pin DDR3 SDRAM Unbuffered SO-DIMM

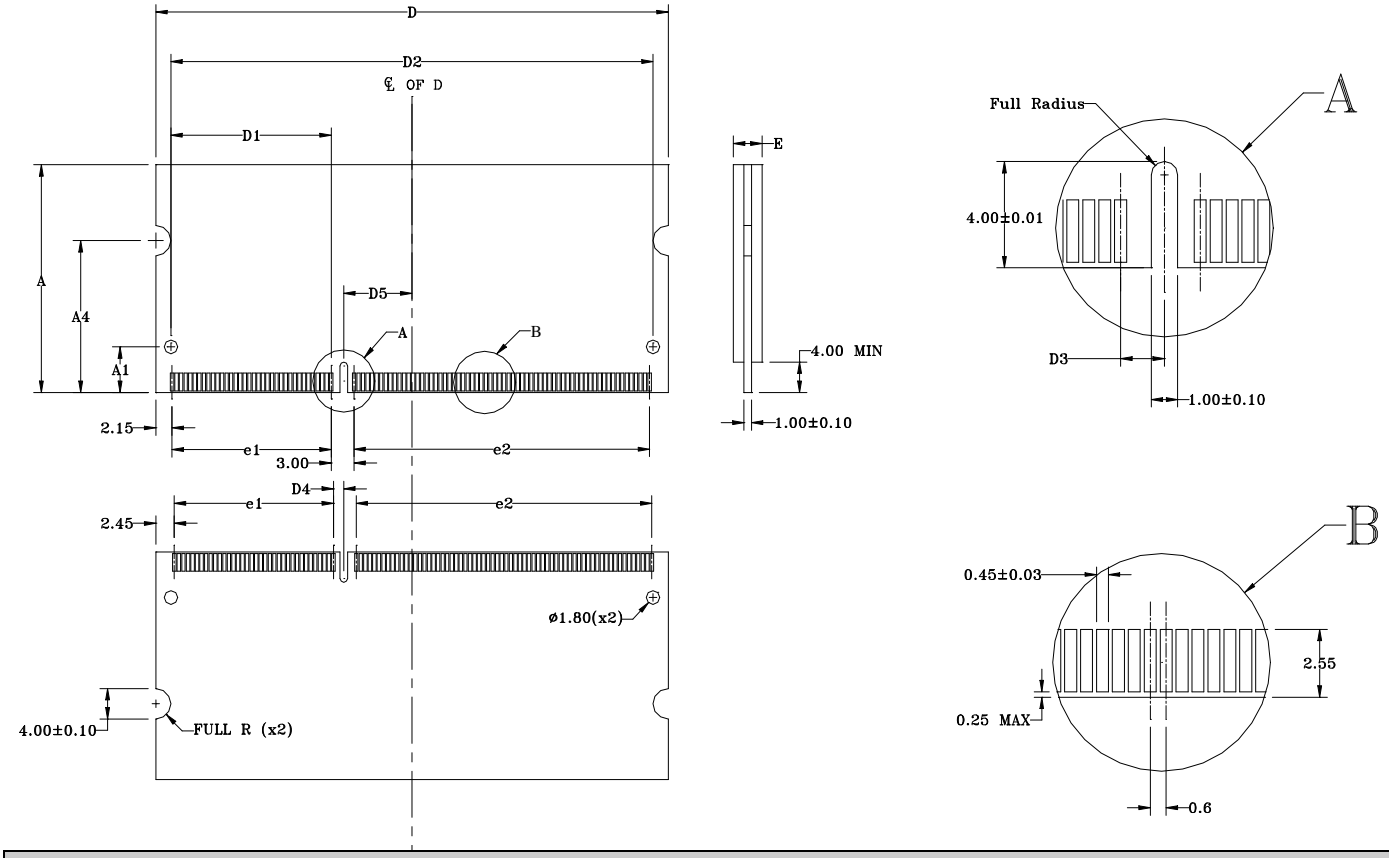


Table 9 - PCB Dimension			
Symbol	MIN	NOM	MAX
A	29.85	30.00	30.15
A1		6.00 Basic	
A4		20.00 Basic	
D	67.45	67.60	67.75
D2		63.60 Basic	
D3		1.65 Basic	
D5		9.00 Basic	
e1		21.00 Basic	
e2		39.00 Basic	
E			3.80

Notes:

- All dimensioning and tolerancing conform to ASME Y14.5M-1994.
- Tolerances for all dimensions ±0.15 unless otherwise specified.
- All dimensions are in millimeters.

Figure 2 – Functional Block Diagram (Page 1 of 3)

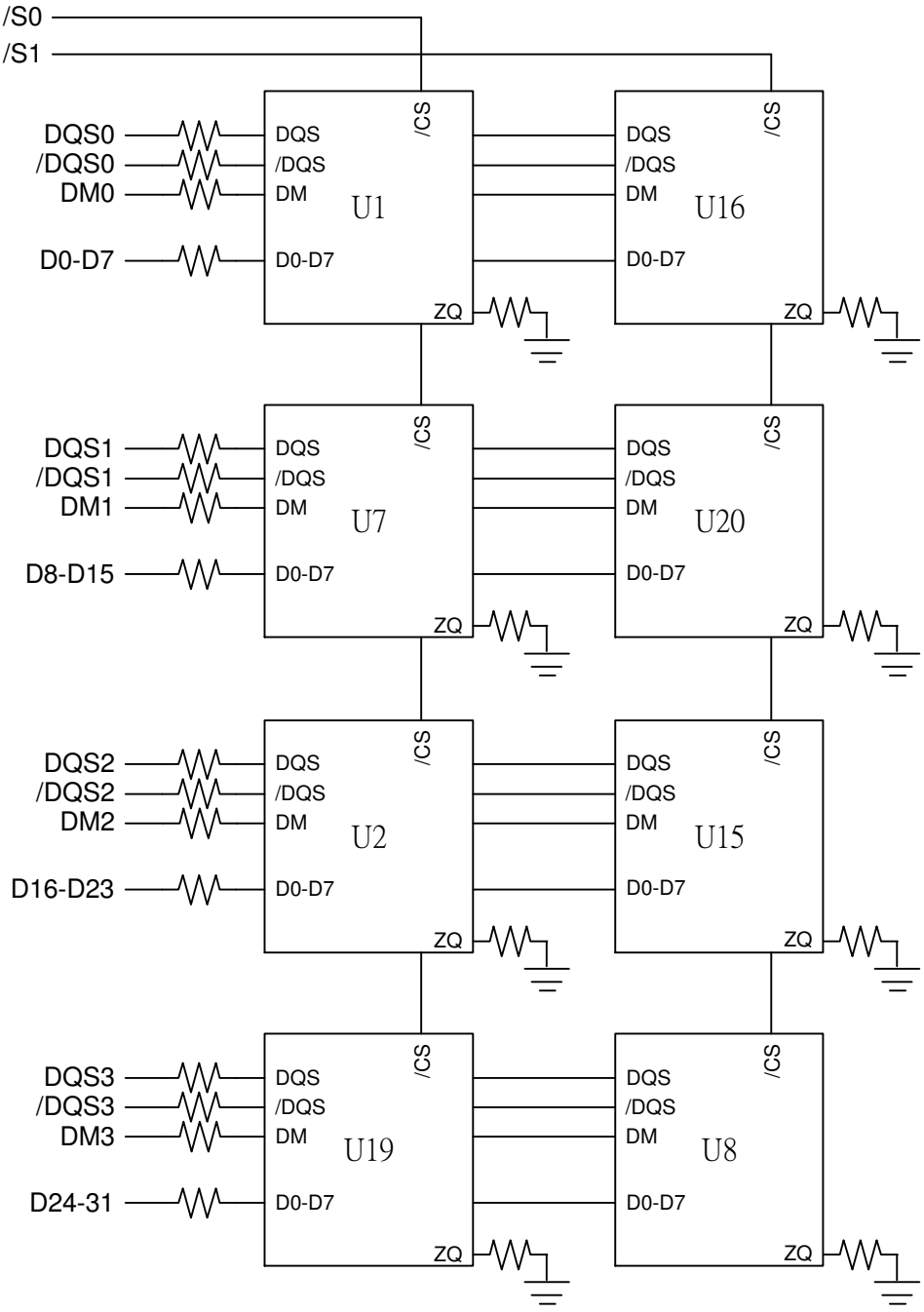


Figure 3 – Functional Block Diagram (Page 2 of 3)

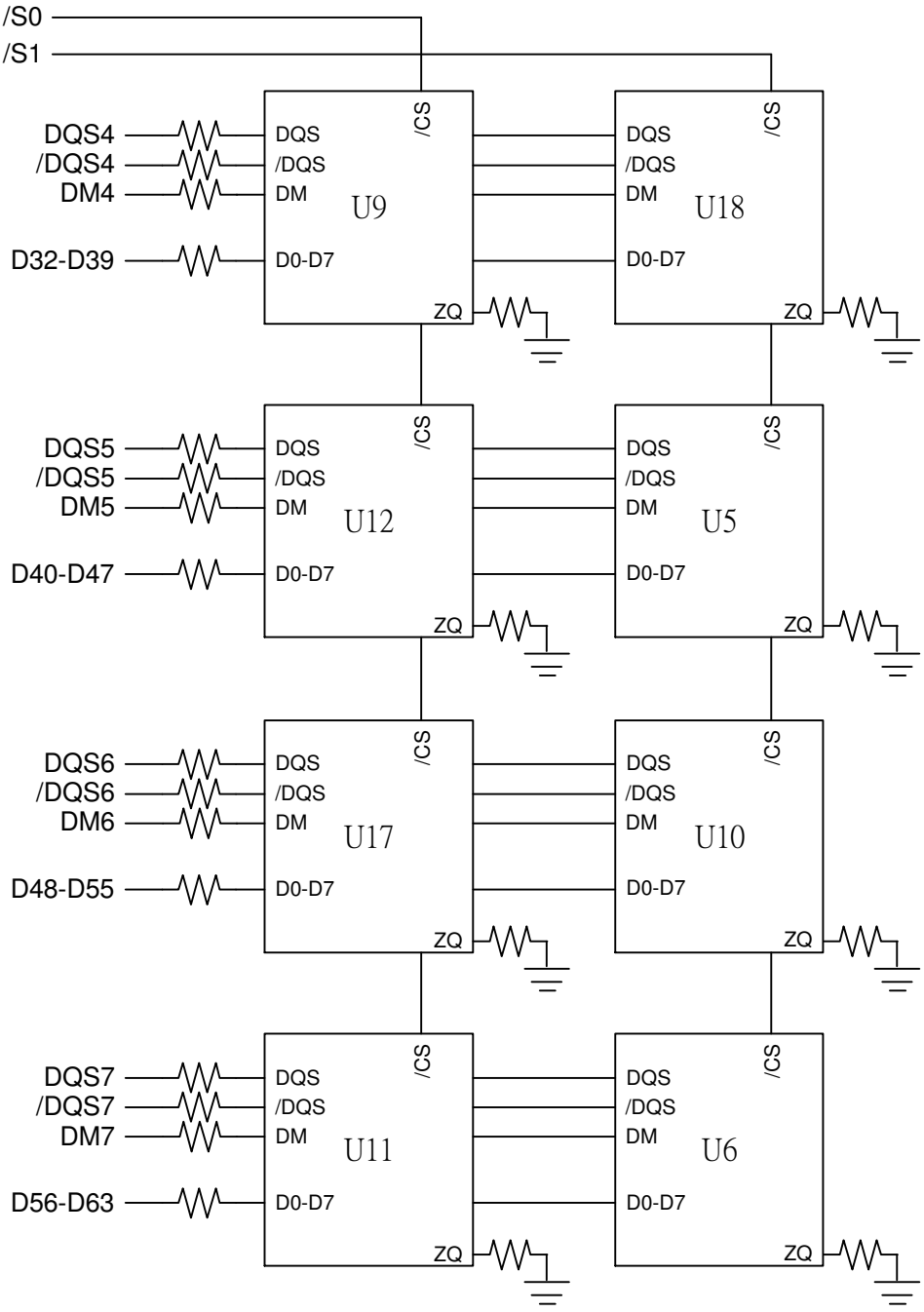
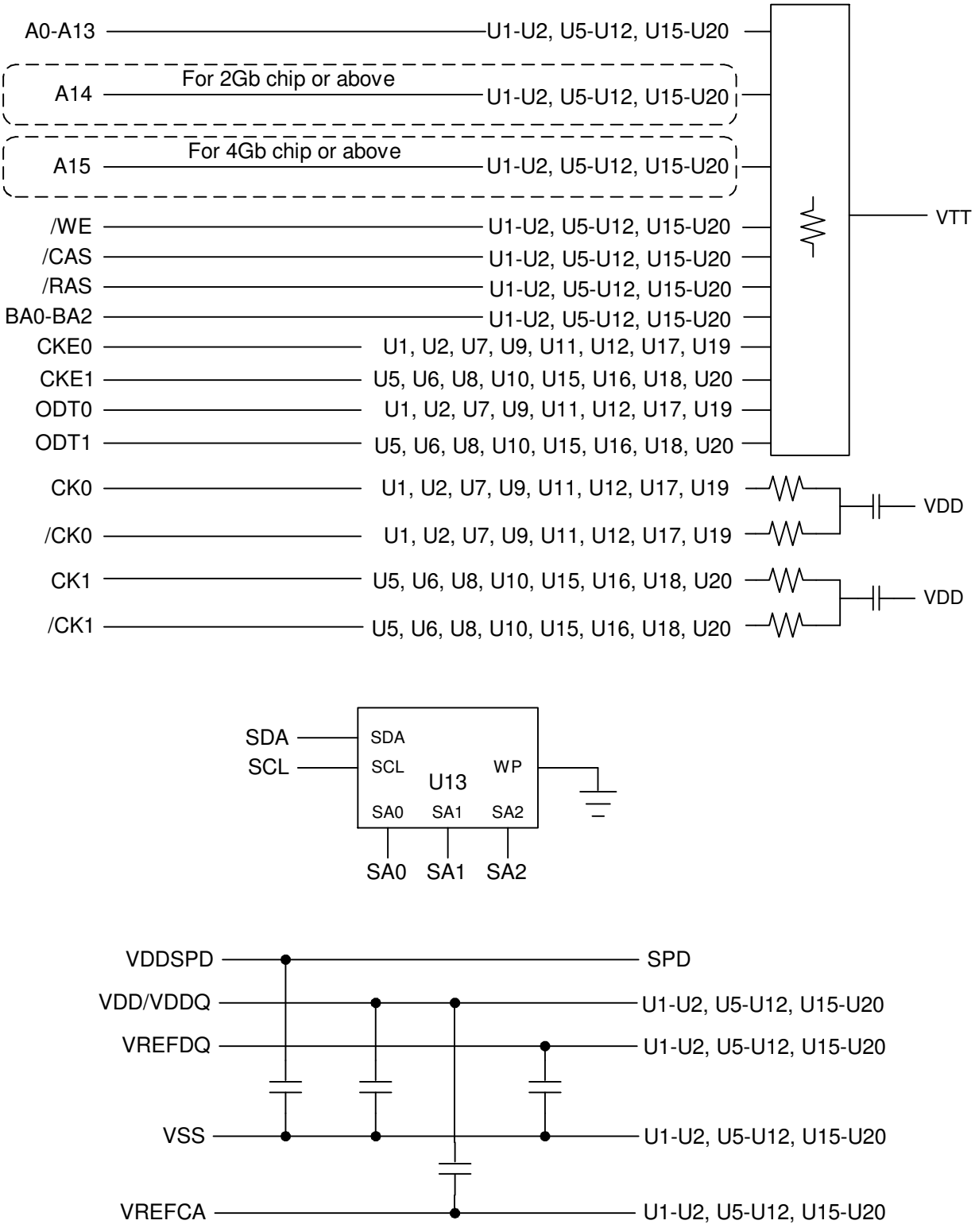


Figure 4 – Functional Block Diagram (Page 3 of 3)



Electrical Parameter

Table 10 - Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on V_{DD}, pin relative to V_{SS}	V_{DD}	-0.4V ~ 1.975	V	1,3
Voltage on V_{DDQ}, pin relative to V_{SS}	V_{DDQ}	-0.4V ~ 1.975	V	1,3
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	-0.4V ~ 1.975	V	1
DRAM Storage temperature	T_{STG}	-55 ~ 100	°C	1,2
DRAM Operation temperature for Commercial temperature product	T_{case}	0 ~ 95	°C	2,4,5
DRAM Operation temperature for Industrial temperature product	T_{case}	-40 ~ 95	°C	2,4,5

Notes:

1 Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2 Storage Temperature or DRAM operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

3 V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REF} must not be greater than 0.6 x V_{DDQ}, when V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.

4 The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85 °C under all operating conditions.

5 Some applications require operation of the Extended Temperature Range between 85 °C and 95 °C case temperature. Full Specifications are guaranteed in this range but the following additional conditions apply a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us. b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

Table 11 - DC Electrical Characteristics and Operating Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ	Max		
Supply voltage	V_{DD}	1.283	1.35	1.45	V	1,2
I/O supply voltage	V_{DDQ}				V	1,2
Supply voltage	V_{DD}	1.425	1.5	1.575	V	1,2,3
I/O supply voltage	V_{DDQ}				V	1,2,3

Notes:

1. V_{DD} and V_{DDQ} must track one another. V_{DDQ} must be less than or equal to V_{DD}. V_{SS} = V_{SSQ}.
2. V_{DD} and V_{DDQ} may include AC noise of +/-50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. V_{DD} and V_{DDQ} must be at same level for valid AC timing parameters.
3. Module is backward-compatible with 1.5V operation.

Table 12 - DC Electrical Characteristics and Input Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ	Max		
V_{IN} low; DC/commands/address buses (1.35V)	V_{IL}	V_{SS}	-	-0.090	V	
V_{IN} low; DC/commands/address buses (1.5V)	V_{IL}	V_{SS}	-	-0.100	V	
V_{IN} high; DC/commands/address buses (1.35V)	V_{IH}	0.090	-	V_{DD}	V	
V_{IN} high; DC/commands/address buses (1.5V)	V_{IH}	0.100	-	V_{DD}	V	
Input reference voltage; command/address bus	$V_{REFCA(DC)}$	0.49* V_{DD}	0.50* V_{DD}	0.51* V_{DD}	V	1,2
I/O reference voltage DQ bus	$V_{REFDQ(DC)}$	0.49* V_{DD}	0.50* V_{DD}	0.51* V_{DD}	V	2,3
Command/address termination voltage (system level, not direct DRAM input)	V_{TT}	-	0.50* V_{DDq}	-	V	4

Notes:

1. $V_{REFCA(DC)}$ is expected to be approximately 0.5 × V_{DD} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFCA} may not exceed ±1% × V_{DD} around the $V_{REFCA(DC)}$ value. Peak-to-peak AC noise on V_{REFCA} should not exceed ±2% of $V_{REFCA(DC)}$.
2. DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20 MHz in frequency.
3. $V_{REFDQ(DC)}$ is expected to be approximately 0.5 × V_{DD} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFDQ} may not exceed ±1% × V_{DD} around the $V_{REFDQ(DC)}$ value. Peak-to-peak AC noise on V_{REFDQ} should not exceed ±2% of $V_{REFDQ(DC)}$.
4. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors. MIN and MAX values are system-dependent.

Table 13 - Input Switching Conditions				
Parameter / Condition	Symbol	Value		Units
		1.35V	1.5V	
Command and Address				
Input high AC voltage: Logic 1 @ 175mV	$V_{IH(AC175)min}$	-	175	mV
Input high AC voltage: Logic 1 @ 160mV	$V_{IH(AC160)min}$	160	-	mV
Input high AC voltage: Logic 1 @ 150mV	$V_{IH(AC150)min}$	-	150	mV
Input high AC voltage: Logic 1 @ 135mV	$V_{IH(AC135)min}$	135	-	mV
Input high DC voltage: Logic 1 @ 100mV	$V_{IH(DC100)min}$	-	100	mV
Input high DC voltage: Logic 1 @ 90mV	$V_{IH(DC90)min}$	90	-	mV
Input low DC voltage: Logic 0 @ -90mV	$V_{IL(DC90)max}$	-90	-	mV
Input low DC voltage: Logic 0 @ -100mV	$V_{IL(DC100)max}$	-	-100	mV
Input low AC voltage: Logic 0 @ -135mV	$V_{IL(AC135)max}$	-135	-	mV
Input low AC voltage: Logic 0 @ -150mV	$V_{IL(AC150)max}$	-	-150	mV
Input low AC voltage: Logic 0 @ -160mV	$V_{IL(AC160)max}$	-160	-	mV
Input low AC voltage: Logic 0 @ -175mV	$V_{IL(AC175)max}$	-	-175	mV

Parameter / Condition	Symbol	Value		Units
		1.35V	1.5V	
DQ and DM				
Input high AC voltage: Logic 1	$V_{IH(AC160)min}$	160	-	mV
Input high AC voltage: Logic 1	$V_{IH(AC150)min}$	-	150	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}$	135	135	mV
Input high DC voltage: Logic 1	$V_{IH(DC100)min}$	-	100	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	-	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)max}$	-90	-	mV
Input low DC voltage: Logic 0	$V_{IL(DC100)max}$	-	-100	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)max}$	-135	-135	mV
Input low AC voltage: Logic 0	$V_{IL(AC150)max}$	-	-150	mV
Input low AC voltage: Logic 0	$V_{IL(AC160)max}$	-160	-	mV

Notes:

1. All voltages are referenced to V_{REF}. V_{REF} is V_{REFCA} for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. V_{REF} is V_{REFDQ} for DQ and DM inputs.
2. Input setup timing parameters (tIS and tDS) are referenced at $V_{IL(AC)}/V_{IH(AC)}$, not $V_{REF(DC)}$.
3. Input hold timing parameters (tIH and tDH) are referenced at $V_{IL(DC)}/V_{IH(DC)}$, not $V_{REF(DC)}$.
4. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).

Table 14 - Differential Input Operating Conditions (CK, /CK and DQS, /DQS)

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Differential input voltage logic high - slew (1.35V)	$V_{IH,diff}$	+180	-	mV	1
Differential input voltage logic high - slew (1.5V)	$V_{IH,diff}$	+200	-	mV	1
Differential input voltage logic low - slew (1.35V)	$V_{IL,diff}$	-	-180	mV	1
Differential input voltage logic low - slew (1.5V)	$V_{IL,diff}$	-	-200	mV	1
Differential input voltage logic high	$V_{IH,diff(AC)}$	2* ($V_{IH(AC)}$ - V_{REF})	-	mV	2
Differential input voltage logic low	$V_{IL,diff(AC)}$	-	2* ($V_{IL(AC)}$ - V_{REF})	mV	3
Single-ended high level for strobes (1.35V)	V_{SEH}	V_{DDQ}/2 + 175	-	mV	2
Single-ended high level for CK, /CK (1.35V)		V_{DD}/2 + 175	-	mV	2
Single-ended high level for strobes (1.5V)	V_{SEH}	V_{DDQ}/2 + 175	-	mV	2
Single-ended high level for CK, /CK (1.5V)		V_{DD}/2 + 175	-	mV	2
Single-ended low level for strobes (1.35V)	V_{SEL}	-	V_{DDQ}/2 - 175	mV	3
Single-ended low level for CK, /CK (1.35V)		-	V_{DD}/2 – 175	mV	3
Single-ended low level for strobes (1.5)	V_{SEL}	-	V_{DDQ}/2 - 175	mV	3
Single-ended low level for CK, /CK (1.5V)		-	V_{DD}/2 - 175	mV	3

Notes:

1. Defines slew rate reference points, relative to input crossing voltages.
2. Minimum DC limit is relative to single-ended signals; overshoot specifications are applicable.
3. Maximum DC limit is relative to single-ended signals; undershoot specifications are applicable.

Table 15 - Single-Ended Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)}$ = V_{TT} - 0.1 * V_{DDQ} and $V_{OH(AC)}$ = V_{TT} + 0.1 * V_{DDQ} (1.35V)	SRQ_{se}	1.75	5	V/ns	1,2,3
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)}$ = V_{TT} - 0.1 * V_{DDQ} and $V_{OH(AC)}$ = V_{TT} + 0.1 * V_{DDQ} (1.5V)	SRQ_{se}	2.5	5	V/ns	1,2,3
Single-ended DC high-level output voltage	$V_{OH(DC)}$	0.8 * V_{DDQ}		V	1,2
Single-ended DC mid-level output voltage	$V_{OM(DC)}$	0.5 * V_{DDQ}		V	1,2
Single-ended DC low-level output voltage	$V_{OL(DC)}$	0.2 * V_{DDQ}		V	1,2
Single-ended AC high-level output voltage	$V_{OH(AC)}$	V_{TT} + 0.1 * V_{DDQ}		V	1,2
Single-ended AC low-level output voltage	$V_{OL(AC)}$	V_{TT} - 0.1 * V_{DDQ}		V	1,2
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				

Notes:

1. RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (V_{DDQ} = V_{DD}, V_{SSQ} = V_{SS}).
2. V_{TT} = V_{DDQ}/2.
3. The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or all switching the opposite direction. For all other DQ signal switching combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.

Table 16 - Differential Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)}$, = - 0.2 * V_{DDQ} and $V_{OH,diff(AC)}$ = + 0.2 * V_{DDQ} (1.35V)	SRQ_{diff}	3.5	12	V/ns	1
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)}$, = - 0.2 * V_{DDQ} and $V_{OH,diff(AC)}$ = + 0.2 * V_{DDQ} (1.5V)	SRQ_{diff}	5	10	V/ns	1
Differential high-level output voltage	$V_{OH,diff(AC)}$	+0.2 * V_{DDQ}		V	1
Differential low-level output voltage	$V_{OL,diff(AC)}$	-0.2 * V_{DDQ}		V	1
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				

Notes:

1. RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (V_{DDQ} = V_{DD}, V_{SSQ} = V_{SS}).
2. V_{REF} = V_{DDQ}/2; slew rate @ 5V/ns, interpolate for faster slew rate.

For part number IMM2G64D3LSOD8AG-C125(I)

Table 17 - IDD Specifications with Conditions and Operation Current

Parameter / Condition	Symbol	Current	Units	Notes
Operating current 0; One bank ACTIVATE-to-PRECHARGE	I_{DD0}	1112	mA	1, 2
Operating current 1; One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	1320	mA	1, 2
Precharge power-down current; Slow exit	I_{DD2P0}	416	mA	1, 3
Precharge power-down current; Fast exit	I_{DD2P1}	800	mA	1, 3
Precharge quiet standby current	I_{DD2Q}	1088	mA	1, 3
Precharge standby current	I_{DD2N}	704	mA	1, 3
Precharge standby ODT current	I_{DD2NT}	1088	mA	1, 3
Active power-down current	I_{DD3P}	896	mA	1, 3
Active standby current	I_{DD3N}	1152	mA	1, 3
Burst read operating current	I_{DD4R}	1912	mA	1, 2
Burst write operating current	I_{DD4W}	2040	mA	1, 2
Refresh current	I_{DD5B}	3848	mA	1, 2
Self refresh temperature current: MAX T_c = 85°C	I_{DD6}	480	mA	1, 3
Self refresh temperature current (SRT-enabled): MAX T_c = 95°C	I_{DD6ET}	640	mA	1, 3
All banks interleaved read current	I_{DD7}	3152	mA	1, 2
Reset current	I_{DD8}	368	mA	1, 3

Notes:

1 Value shown for DDR3 SDRAM only and are computed from values specified in the 8Gbit component data sheet.

2 One module rank in the active IDD, the other rank in IDD2N.

3 All ranks in this IDD conditions.

For part number IMM2G64D3LSOD8AG-C125(I)

Table 18 - AC Timing Parameter and Operating Conditions

Parameter / Condition		Symbol	Min	Max	Units
Clock Timing					
Clock period average: DLL disable mode	T_C = 0°C to 85°C	^tCK (DLL_DIS)	8	-	ns
	T_C => 85°C to 95°C		8	-	
Clock periods average: DLL enable mode (CL = 11, CWL = 8)		^tCK (AVG)	1.25	<1.5	ns
Clock periods average: DLL enable mode (CL = 9, CWL = 7)		^tCK (AVG)	1.5	<1.875	ns
High pulse width average		^tCH (AVG)	0.47	0.53	^tCK
Low pulse width average		^tCL (AVG)	0.47	0.53	^tCK
Clock period jitter	DLL locked	^tJITper	-70	70	ps
	DLL locking	$^tJITper,Ick$	-60	60	ps
Clock absolute period		^tCK (ABS)	^tCK (AVG) MIN + ^tJITper MIN	^tCK (AVG) MAX + ^tJITper MAX	ps
Clock absolute high pulse width		^tCH (ABS)	0.43	-	^tCK (AVG)
Clock absolute low pulse width		^tCL (ABS)	0.43	-	^tCK (AVG)
Cycle-to-cycle jitter	DLL locked	^tJITcc	140		ps
	DLL locking	$^tJITcc,Ick$	120		ps
Cumulative error across	2 cycles	$^tERR2per$	-103	103	ps
	3 cycles	$^tERR3per$	-122	122	ps
	4 cycles	$^tERR4per$	-136	136	ps
	5 cycles	$^tERR5per$	-147	147	ps
	6 cycles	$^tERR6per$	-155	155	ps
	7 cycles	$^tERR7per$	-163	163	ps
	8 cycles	$^tERR8per$	-169	169	ps
	9 cycles	$^tERR9per$	-175	175	ps
	10 cycles	$^tERR10per$	-180	180	ps
	11 cycles	$^tERR11per$	-184	184	ps
	12 cycles	$^tERR12per$	-188	188	ps
	n = 14,…49, 50 cycles	$^tERRnper$	(1+0.68ln[n]) * ^tJITper MIN	(1+0.68ln[n]) * ^tJITper Max	ps
DQ Input Timing					
Data setup time to DQS, /DQS (1.35V)	Base (specification)	^tDS (AC135)	25	-	ps
					ps
Data setup time to DQS, /DQS (1.5V)	Base (specification)	^tDS (AC150)	10	-	ps
					ps
Data hold time from DQS, /DQS (1.35V)	Base (specification)	^tDH (DC90)	55	-	ps
					ps
Data hold time from DQS, /DQS (1.5V)	Base (specification)	^tDH (DC100)	45	-	ps
					ps
Minimum data pulse width		^tDIPW	360	-	ps
DQ Output Timing					
DQS, /DQS to DQ skew, per access		^tDQSQ	-	100	ps
DQ output hold time from DQS, /DQS		^tQH	0.38	-	^tCK (AVG)
DQ Low-Z time from CK, /CK		^tLZDQ	-450	225	ps
DQ High-Z time from CK, /CK		^tHZDQ	-	225	ps
DQ Strobe Input Timing					
DQS, /DQS rising to CK, /CK rising		^tDQSS	-0.27	0.27	^tCK
DQS, /DQS differential input low pulse width		^tDQSL	0.45	0.55	^tCK

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Parameter / Condition		Symbol	Min	Max	Units
DQS, /DQS falling setup to CK, /CK rising		tDSS	0.18	-	tCK
DQS, /DQS falling hold from CK, /CK rising		tDSH	0.18	-	tCK
DQS, /DQS differential input high pulse width		tDQSH	0.45	0.55	tCK
DQS, /DQS differential WRITE preamble		tWPRE	0.9	-	tCK
DQS, /DQS differential WRITE postamble		tWPST	0.3	-	tCK
DQ Strobe Output Timing					
DQS, /DQS rising to/from CK, /CK		tDQSCK	-225	225	ps
DQS, /DQS differential output high time		tQSH	0.40	-	tCK
DQS, /DQS differential output low time		tQSL	0.40	-	tCK
DQS, /DQS Low-Z time (RL-1)		tLZDQS	-450	225	ps
DQS, /DQS High-Z time (RL+BL/2)		tHZDQS	-	225	ps
DQS, /DQS differential READ preamble		tRPRE	0.9	greater of tLZ(DQS)(MIN)or tDQSK(DQS)(MAX)	tCK
DQS, /DQS differential READ postamble		tRPST	0.3	greater of tDQSCK(MIN) + tQSH(MIN) or tHZ(DQS)(MAX)	tCK
Command and Address Timing					
DLL locking time		tDLLK	512	-	tCK
CTRL, CMD, ADDR setup to CK, /CK (1.35V)	Base (specification)	tIS (AC160)	60	-	ps
					ps
CTRL, CMD, ADDR setup to CK, /CK (1.35V)	Base (specification)	tIS (AC135)	185	-	ps
					ps
CTRL, CMD, ADDR setup to CK, /CK (1.5V)	Base (specification)	tIS (AC175)	45	-	ps
				-	ps
CTRL, CMD, ADDR setup to CK, /CK (1.5V)	Base (specification)	tIS (AC150)	170	-	ps
					ps
CTRL, CMD, ADDR hold from CK, /CK (1.35V)	Base (specification)	tIH (DC90)	130	-	ps
					ps
CTRL, CMD, ADDR hold from CK, /CK (1.5V)	Base (specification)	tIH (DC100)	120	-	ps
					ps
Minimum CTRL, CMD, ADDR pulse width		tIPW	560	-	ps
ACTIVATE to internal READ or WRITE delay		tRCD	13.125	-	ns
PRECHARGE command period		tRP	13.125	-	ns
ACTIVATE-to-PRECHARGE command period		tRAS	35	9 * tREFI	ns
ACTIVATE-to-ACTIVATE command period		tRC	48.125	-	ns
ACTIVATE-to-ACTIVATE minimum period		tRRD	greater of 4tCK or 6ns	-	tCK
Four ACTIVATE windows (1KB page size)		tFAW	40	-	ns
Write recovery time		tWR	15	-	ns
Delay from start of internal WRITE transaction to internal READ command		tWTR	greater of 4tCK or 7.5ns	-	tCK
READ-to-PRECHARGE time		tRTP	greater of 4tCK or 7.5ns	-	tCK
/CAS-to-/CAS command delay		tCCD	4tCK	-	tCK
Auto precharge write recovery + precharge time		tDAL	WR + tRP/tCK (AVG)	-	tCK
MODE REGISTER SET command cycle time		tMRD	4	-	tCK
MODE REGISTER SET command update delay		tMOD	greater of 12tCK or 15ns	-	tCK
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		tMPRR	1	-	tCK

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Parameter / Condition		Symbol	Min	Max	Units
Calibration Timing					
ZQCL command: Long calibration time	POWER-UP and RESET operation	tZQinit	512	-	tCK
	Normal operation	tZQoper	256	-	tCK
ZQCS command: Short calibration time		tZQcs	64	-	tCK
Initialization and Reset Timing					
Exit reset from CKE HIGH to valid command		tXPR	greater of 5tCK or tRFC(min)+10ns	-	tCK
Refresh Timing					
REFRESH-to-ACTIVATE or REFRESH command period		tRFC	300	-	ns
Maximum refresh period	T_C<=85ºC	-	64 (1X)		ms
	T_C>85ºC		32 (2X)		
Maximum average periodic refresh	T_C<=85ºC	tREFI	7.8 (64ms/8192)		us
	T_C>85ºC		3.9 (32ms/8192)		
Self Refresh Timing					
Exit self refresh to commands not requiring a locked DLL		tXS	greater of 5 tCK or tRFC+10ns	-	tCK
Exit self refresh to commands requiring a locked DLL		tXSDLL	tDLLK (MIN)	-	tCK
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		tCKESR	tCKE (MIN) + tCK	-	tCK
Valid clocks after self refresh entry or power down entry		tCKSRE	greater of 5tCK or 10ns	-	tCK
Valid clocks before self refresh exit, power-down exit, or reset exit		tCKSRX	greater of 5tCK or 10ns	-	tCK
Power-Down Timing					
CKE MIN pulse width		tCKE (MIN)	greater of 3tCK or 5ns		tCK
Command pass disable delay		tCPDED	1	-	tCK
Power-down entry to power exit timing		tPD	tCKE (MIN)	9 * tREFI	tCK
Power-Down Entry Minimum Timing					
ACTIVATE command to power-down entry		tACTPDEN	MIN = 1		tCK
PRECHARGE/PRECHARGE ALL command to power-down entry		tPRPDEN	MIN = 1		tCK
REFRESH command to power-down entry		tREFPDEN	MIN = 1		tCK
MRS command to power-down entry		tMRSPDEN	MIN = tMOD (MIN)		tCK
READ/READ with auto precharge command to power-down entry		tRDPDEN	MIN = RL + 4 + 1		tCK
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	tWRPDEN	MIN = WL + 4 + tWR/tCK (AVG)		tCK
	BC4MRS	tWRPDEN	MIN = WL + 2 + tWR/tCK (AVG)		tCK
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	tWRAPDEN	MIN = WL + 4 + tWR + 1		tCK
	BC4MRS	tWRAPDEN	MIN = WL + 2 + tWR + 1		tCK
Power-Down Exit Timing					
DLL on, any valid command, or DLL off to commands not requiring locked DLL		tXP	greater of 3tCK or 6ns	-	tCK
Precharge power-down with DLL off to commands requiring a locked DLL		tXPDLL	greater of 10tCK or 24ns	--	tCK

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Parameter / Condition	Symbol	Min	Max	Units
ODT Timing				
R_{TT} turn-on from ODTL on reference	^{t}AON	-225	225	ps
R_{TT} turn-off from ODTL off reference	^{t}AOF	0.3	0.7	CK
Asynchronous R_{TT} turn-on delay (power-down with DLL off)	^{t}AONPD	2	8.5	ns
Asynchronous R_{TT} turn-off delay (power-down with DLL off)	^{t}AOFPD	2	8.5	ns
ODT HIGH time with WRITE command and BL8	ODTH8	6	-	^{t}CK
ODT HIGH time without WRITE command or WRITE command and BC4	ODTH4	4	-	^{t}CK
Dynamic ODT Timing				
R_{TT} dynamic change skew	^{t}ADC	0.3	0.7	^{t}CK
Write Leveling Timing				
First DQS, /DQS rising edge	^{t}WLMRD	40	-	^{t}CK
DQS, /DQS delay	^{t}WLDQSEN	25	-	^{t}CK
Write leveling setup from rising CK, /CK crossing to rising DQS, /DQS crossing	^{t}WLS	165	-	ps
Write leveling hold from rising DQS, /DQS crossing to rising CK, /CK crossing	^{t}WLH	165	-	ps
Write leveling output delay	^{t}WLO	0	7.5	ns
Write leveling output error	^{t}WLOE	0	2	ns

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Table 19 - SPD Information

Byte NO.	Description	Note	Hex
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	176 / 256 / 0-116	92
1	SPD Revision	1.2	12
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte / Module Type	64b Unbuffered SO-DIMM	03
4	SDRAM Density and Banks	8Gb 8banks	05
5	SDRAM Addressing	Row 16 / Col 11	22
6	Module Nominal Voltage, V_{DD}	1.35V/1.5V	02
7	Module Organization	2Rank , x8	09
8	Module Memory Bus Width	Non-ECC, 64bit	03
9	Fine Timebase (FTB) Dividend and Divisor	2.5ps	52
10	Medium Timebase (MTB) Dividend	1/8 (0.125ns)	01
11	Medium Timebase (MTB) Divisor	1/8 (0.125ns)	08
12	SDRAM Minimum Cycle Time (tCKmin)	1.25ns	0A
13	Reserved	-	00
14	CAS Latencies Supported, Least Significant Byte	5, 6, 7, 8, 9, 10, 11	FE
15	CAS Latencies Supported, Most Significant Byte	-	00
16	Minimum CAS Latency Time (tAAmin)	13.125ns	69
17	Minimum Write Recovery Time (tWRmin)	15ns	78
18	Minimum /RAS to /CAS Delay Time (tRCDmin)	13.125ns	69
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	7.5ns	3C
20	Minimum Row Precharge Time (tRPmin)	13.125ns	69
21	Upper Nibbles for tRAS and tRC	-	11
22	Minimum Active to Precharge Time (tRASmin), LSB	35ns	18
23	Minimum Active to Active/Refresh Time (tRCmin), LSB	48.125ns	81
24	Minimum Refresh Recovery Time (tRFCmin), LSB	300ns	60
25	Minimum Refresh Recovery Time (tRFCmin), MSB	300ns	09
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	7.5ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns	3C
28	Upper Nibble for tFAW	40ns	01
29	Minimum Four Activate Window Delay Time (tFAWmin), LSB	40ns	40
30	SDRAM Optional Features	DLL off Mode, RZQ/6, RZQ/7	83
31	SDRAM Thermal and Refresh Options	0-95oC Op. Temp. w/2x refresh	05
32	Module Thermal Sensor	Without TS	00
33	SDRAM Device Type	Non-Standard SDRAM	A1
34-59	Reserved, General Section	-	00
60	Module Nominal Height	29< Height <= 30	0F

Byte NO.	Description	Note	Hex
61	Module Maximum Thickness	1< Tf <=2 (mm); 1< Tb <=2 (mm)	11
62	Reference Raw Card Used	Raw Card F3	65
63	Address Mapping from Edge Connector to DRAM	Non-Mirrored	00
64-116	Module Type Specific Section, Indexed by Key Byte	-	00
117-118	Module ID: Module Manufacturer's JEDEC ID Code	Reserved	Reserved
119	Module ID: Module Manufacturing Location	Reserved	Reserved
120-121	Module ID: Module Manufacturing Date	Reserved	Reserved
122-125	Module ID: Module Serial Number	Reserved	Reserved
126-127	Cyclical Redundancy Code	-	2A 50
128-145	Module Part Number	Reserved	Reserved
146-147	Module Revision Code	Reserved	Reserved
148-149	DRAM Manufacturer's JEDEC ID Code	Reserved	Reserved
150-175	Manufacturer's Specific Data	Reserved	Reserved
176-255	Open For Customer Use	Reserved	Reserved

Revision History

Revision	Descriptions	Release Date
1.0	Initial release	Feb, 2018

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