

Datasheet | Rev. 1.0 | 2018

IMM2G72D3LRVQ8AG (Die Revision C) 16GByte (2048M x 72 Bit)

16GB DDR3 VLP Registered DIMM
RoHS Compliant Product

Remark:

Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures .

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Features

- 240-Pin Registered Dual-In-Line Memory Module
- Capacity: 16GB
- JEDEC-Standard
- Bi-directional Differential Data-Strobe
- 72 Bit Data Bus Width with ECC
- Programmable CAS Latency (CL):
 - PC3-12800: 5, 6, 7, 8, 9, 10, 11
 - PC3-10600: 5, 6, 7, 8, 9, 10
- Programmable CAS Write Latency (CWL):
 - PC3-12800: 5, 6, 7, 8
 - PC3-10600: 5, 6, 7
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- On-Die Termination (ODT)
- ZQ Calibration Supported
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Asynchronous Reset
- On-board I2C Temperature Sensor with Integrated Serial Presence Detect (SPD) EEPROM
- Gold Edge Contacts
- 100% RoHS-Compliant
- Very Low Profile Module Height: 18.75mm (0.738 inch)

Table 1 - Ordering Information for RoHS Compliant Product

Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM2G72D3xRVQ8AG-Czzzy	16GB	2Gx72	4	16GB DDR3 VLP Registered DIMM

Notes:
 x: Operating Voltage
 y: Operating Temperature
 zzz: Speed Grade

Table 2 - Operating Voltage

Part Number	Operating Voltage
L	V _{DD} , V _{DDQ} = 1.35V (1.283V-1.45V) Backward compatible to V _{DD} , V _{DDQ} = 1.5V (1.425V-1.575V)

Table 3 - Temperature Grade

Part Number	Temperature Grade	T _{case}
Blank	Commercial temperature	0°C to 95°C
I	Industrial temperature	-40°C to 95°C

Remark: T_{case} is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85 °C < T_{case} <= 95 °C.

Table 4 - Speed Grade

Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
125	PC3-12800 (DDR3-1600)	800MHz (1.25ns@CL=11)
15E	PC3-10600 (DDR3-1333)	667MHz (1.5ns@CL=9)

Table 5 - Memory Chip Information

Part Number	Base Device Brand	Base device	Voltage	Type	Chip Packing
IMM2G72D3LRVQ8AG-Czzzy	I'M	IM8G08D3FCDG	1.35V	512Mx8x2 DDP	Lead Free

Part Number Decoder

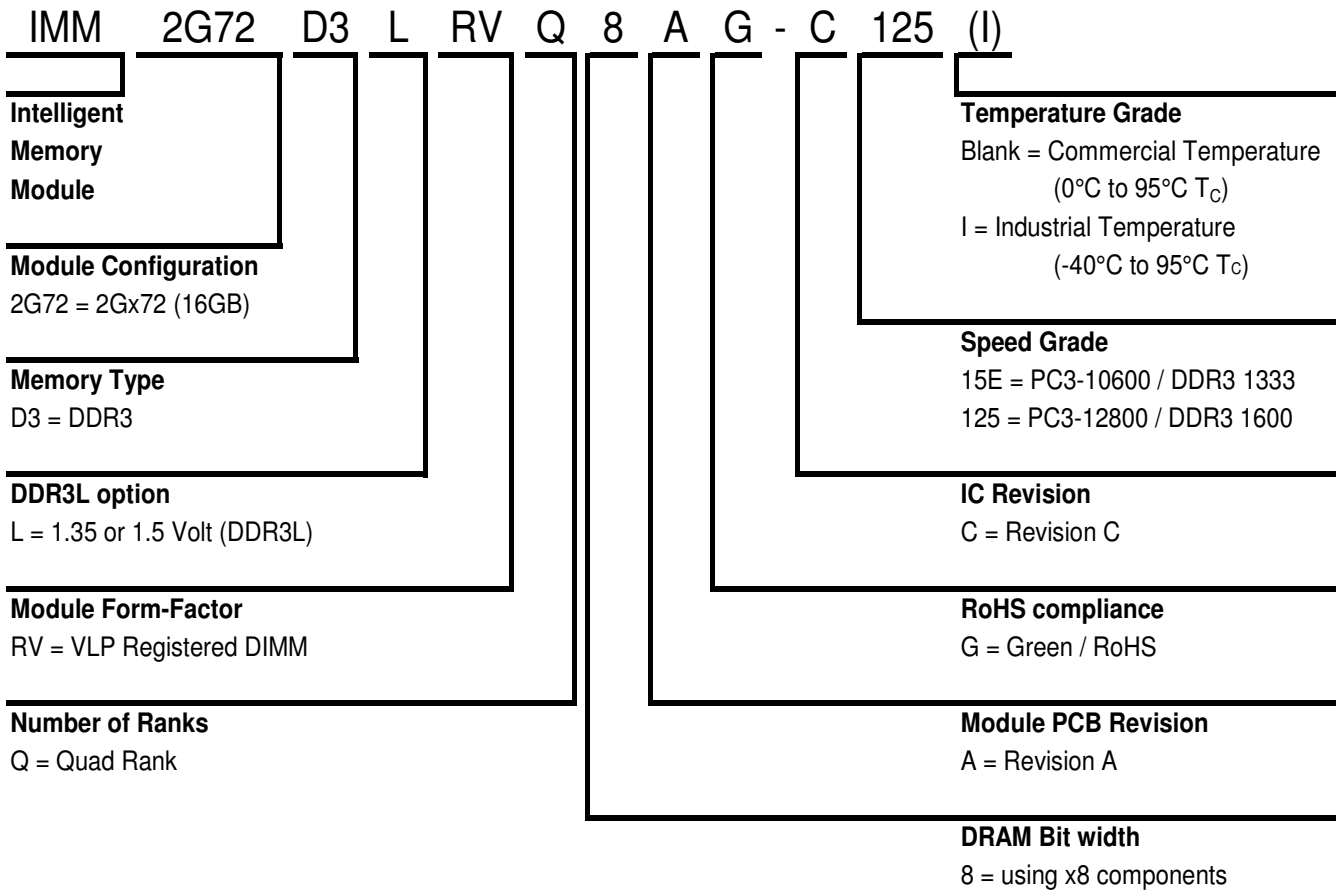


Table 6 - Addressing

Parameter	16GB
Refresh count	8K
Row address	64K A[15:0]
Device bank address	8 BA[2:0]
Device configuration	8Gb (512Mx8x2 DDP)
Column address	1K A[9:0]
Module rank address	4 /S[3:0]
Number of devices	18

Table 7 - Pin Assignment

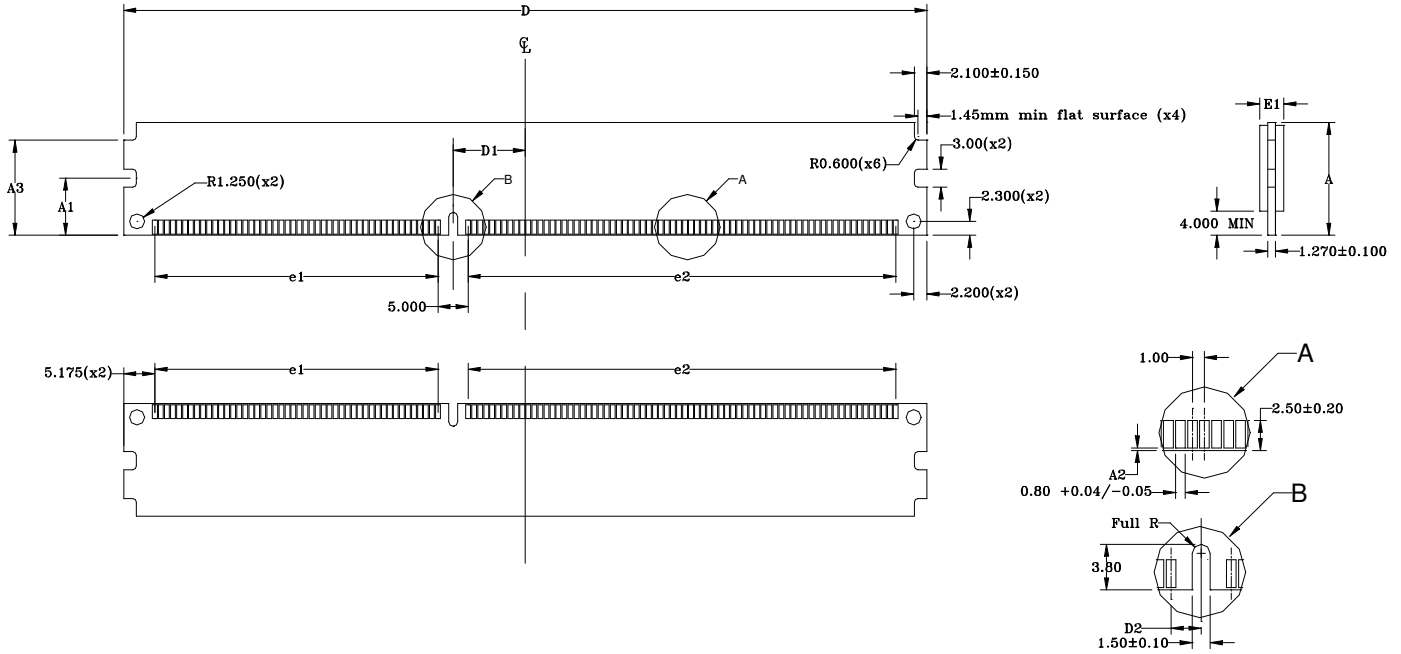
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V _{REFDQ}	121	V _{SS}	61	A2	181	A1
2	V _{SS}	122	D4	62	V _{DD}	182	V _{DD}
3	D0	123	D5	63	CK1	183	V _{DD}
4	D1	124	V _{SS}	64	/CK1	184	CK0
5	V _{SS}	125	DM0, TDQS9	65	V _{DD}	185	/CK0
6	/DQS0	126	NC, /TDQS9	66	V _{DD}	186	V _{DD}
7	DQS0	127	V _{SS}	67	V _{REFCA}	187	/EVENT
8	V _{SS}	128	D6	68	PAR_IN	188	A0
9	D2	129	D7	69	V _{DD}	189	V _{DD}
10	D3	130	V _{SS}	70	A10, AP	190	BA1
11	V _{SS}	131	D12	71	BA0	191	V _{DD}
12	D8	132	D13	72	V _{DD}	192	/RAS
13	D9	133	V _{SS}	73	/WE	193	/S0
14	V _{SS}	134	DM1, TDQS10	74	/CAS	194	V _{DD}
15	/DQS1	135	NC, /TDQS10	75	V _{DD}	195	ODT0
16	DQS1	136	V _{SS}	76	/S1	196	A13
17	V _{SS}	137	D14	77	ODT1	197	V _{DD}
18	D10	138	D15	78	V _{DD}	198	/S3
19	D11	139	V _{SS}	79	/S2	199	V _{SS}
20	V _{SS}	140	D20	80	V _{SS}	200	D36
21	D16	141	D21	81	D32	201	D37
22	D17	142	V _{SS}	82	D33	202	V _{SS}
23	V _{SS}	143	DM2, TDQS11	83	V _{SS}	203	DM4, TDQS13
24	/DQS2	144	NC, /TDQS11	84	/DQS4	204	NC, /TDQS13
25	DQS2	145	V _{SS}	85	DQS4	205	V _{SS}
26	V _{SS}	146	D22	86	V _{SS}	206	D38
27	D18	147	D23	87	D34	207	D39
28	D19	148	V _{SS}	88	D35	208	V _{SS}
29	V _{SS}	149	D28	89	V _{SS}	209	D44
30	D24	150	D29	90	D40	210	D45
31	D25	151	V _{SS}	91	D41	211	V _{SS}
32	V _{SS}	152	DM3, TDQS12	92	V _{SS}	212	DM5, TDQS14
33	/DQS3	153	NC, /TDQS12	93	/DQS5	213	NC, /TDQS14
34	DQS3	154	V _{SS}	94	DQS5	214	V _{SS}
35	V _{SS}	155	D30	95	V _{SS}	215	D46
36	D26	156	D31	96	D42	216	D47
37	D27	157	V _{SS}	97	D43	217	V _{SS}
38	V _{SS}	158	CB4	98	V _{SS}	218	D52
39	CB0	159	CB5	99	D48	219	D53
40	CB1	160	V _{SS}	100	D49	220	V _{SS}
41	V _{SS}	161	DM8, TDQS17	101	V _{SS}	221	DM6, TDQS15
42	/DQS8	162	NC, /TDQS17	102	/DQS6	222	NC, /TDQS15
43	DQS8	163	V _{SS}	103	DQS6	223	V _{SS}
44	V _{SS}	164	CB6	104	V _{SS}	224	D54
45	CB2	165	CB7	105	D50	225	D55
46	CB3	166	V _{SS}	106	D51	226	V _{SS}
47	V _{SS}	167	NC	107	V _{SS}	227	D60
48	V _{TT}	168	/RESET	108	D56	228	D61
49	V _{TT}	169	CKE1	109	D57	229	V _{SS}
50	CKE0	170	V _{DD}	110	V _{SS}	230	DM7, TDQS16
51	V _{DD}	171	A15	111	/DQS7	231	NC, /TDQS16
52	BA2	172	A14	112	DQS7	232	V _{SS}
53	/ERR_OUT	173	V _{DD}	113	V _{SS}	233	D62
54	V _{DD}	174	A12, /BC	114	D58	234	D63
55	A11	175	A9	115	D59	235	V _{SS}
56	A7	176	V _{DD}	116	V _{SS}	236	V _{DDSPD}
57	V _{DD}	177	A8	117	SA0	237	SA1
58	A5	178	A6	118	SCL	238	SDA
59	A4	179	V _{DD}	119	SA2	239	V _{SS}
60	V _{DD}	180	A3	120	V _{TT}	240	V _{TT}

Table 8 - Pin Description

Pin Name	Description	Pin Name	Description
V _{DD}	SDRAM core power supply	V _{REFDQ}	SDRAM I/O reference supply
V _{REFCA}	SDRAM command/address reference supply	V _{SS}	Power supply return (ground)
A0-A15	SDRAM address bus	BA0-BA2	SDRAM bank addresses
CK0-CK1	SDRAM clocks (positive line of differential pair)	/CK0-/CK1	SDRAM clocks (negative line of differential pair)
/RAS	SDRAM row address strobe	/CAS	SDRAM column address strobe
/WE	SDRAM write enable	CKE0-CKE1	SDRAM clock enable lines
/S0-/S3	DIMM Rank Select Lines	ODT0-ODT1	On-die termination control lines
DQS0-DQS8	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS8	SDRAM data strobes (negative line of differential pair)
TDQS9-TDQS17	Termination SDRAM data strobes (positive line of differential pair)	/TDQS9-/TDQS17	Termination SDRAM data strobes (negative line of differential pair)
D0-D63	DIMM memory data bus	CB0-CB7	Data check bits Input/Output
DM0-DM8	Data Masks	SDA	EEPROM data line
SCL	EEPROM clock	V _{DDSPD}	EEPROM positive power supply
SA0-SA2	EEPROM address input	/EVENT	Temperature event
PAR_IN	Parity Input	/RESET	Register and SDRAM control pin
/ERR_OUT	Parity Error Output	V _{TT}	Termination Voltage
NC	Spare Pins (no connect)	-	-

Module Dimension

Figure 1 – 240 Pin DDR3 SDRAM VLP Registered DIMM



Symbol	MIN	NOM	MAX
A	18.60	18.75	18.90
A1	9.35	9.50	9.65
A2	0.05	0.20	0.35
A3	15.65	15.80	15.95
D	133.20	133.35	133.50
D1	12.00 Basic		
D2	2.50 Basic		
e1	47.00 Basic		
e2	71.00 Basic		
E1			4.00

Notes:

- All dimensioning and tolerancing conform to ASME Y14.5M-1994.
- Tolerances for all dimensions ±0.15 unless otherwise specified.
- All dimensions are in millimeters.

Figure 2 – Functional Block Diagram (Page 1 of 3)

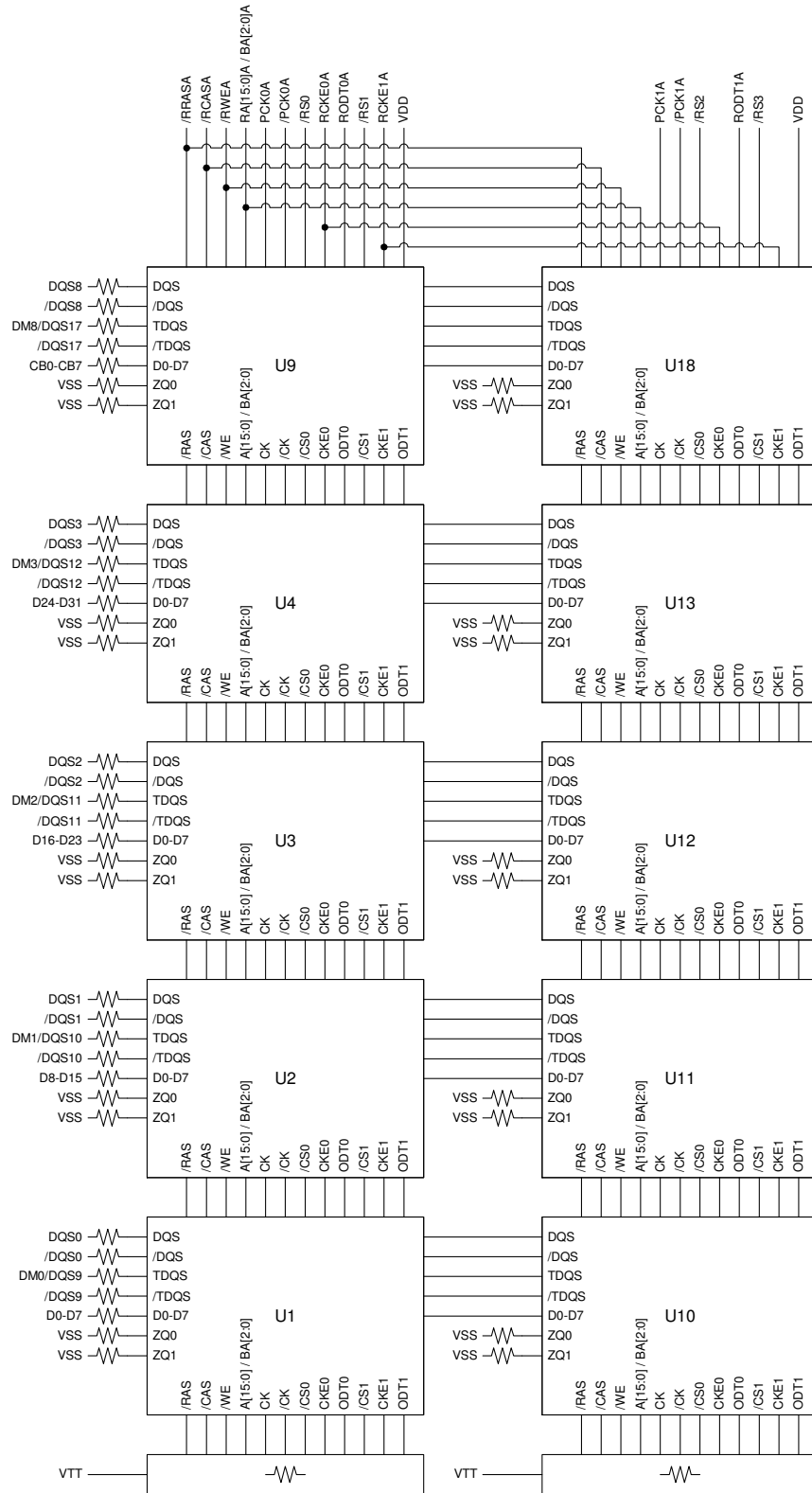


Figure 3 – Functional Block Diagram (Page 2 of 3)

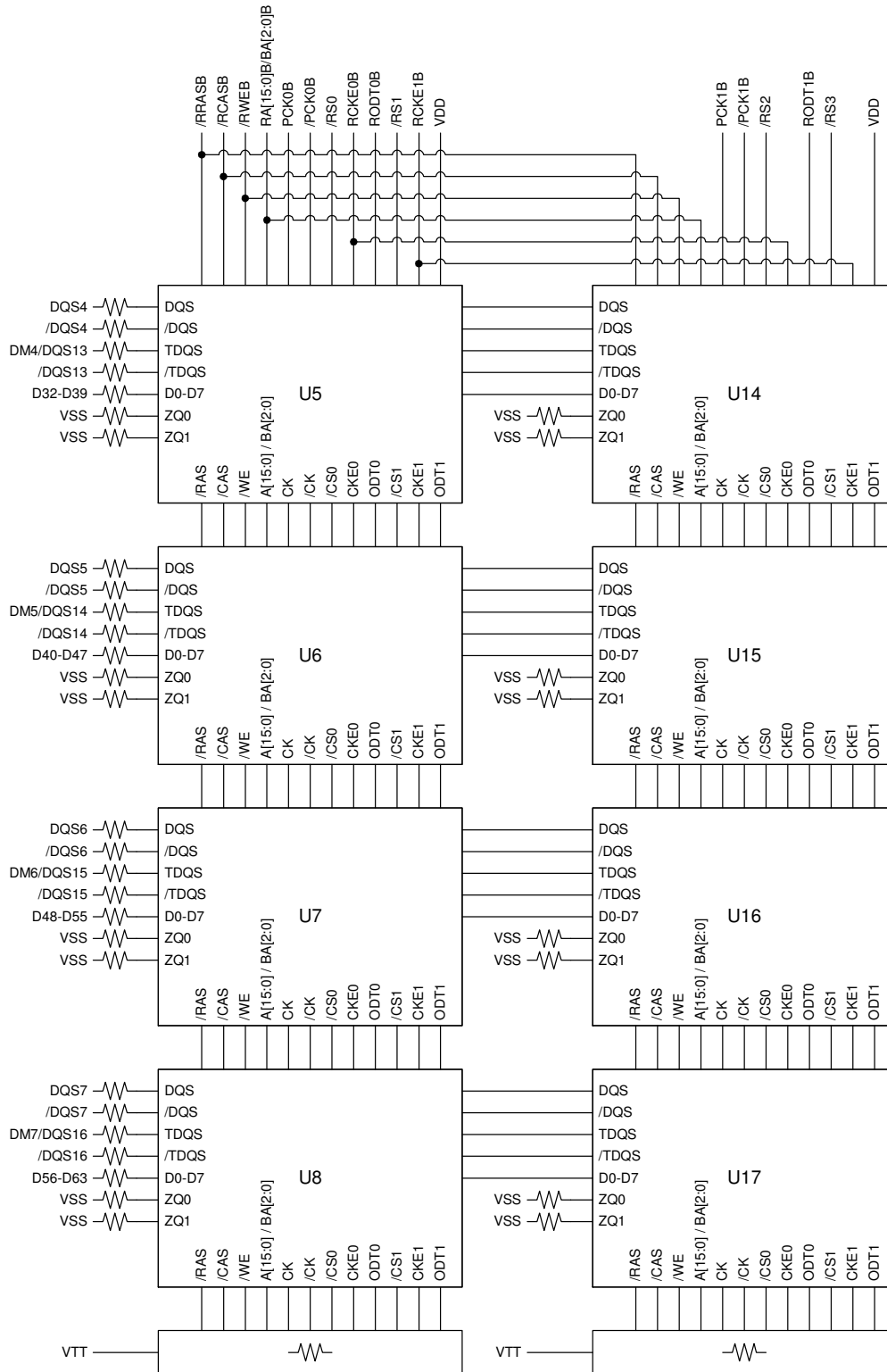
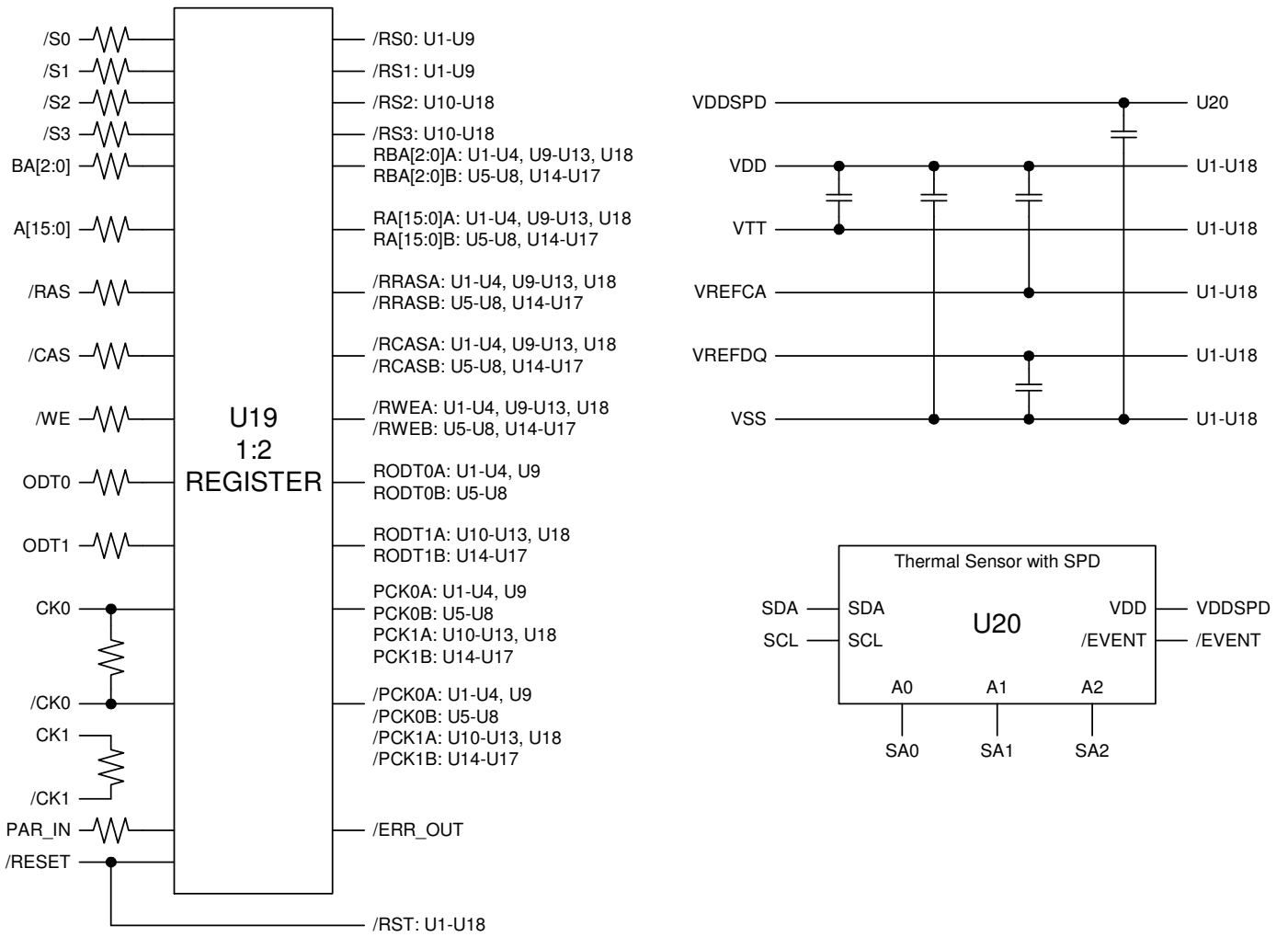


Figure 4 – Functional Block Diagram (Page 3 of 3)



Electrical Parameter

Table 10 - Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on V _{DD} , pin relative to V _{SS}	V _{DD}	-0.4V ~ 1.975	V	1,3
Voltage on V _{DDQ} , pin relative to V _{SS}	V _{DDQ}	-0.4V ~ 1.975	V	1,3
Voltage on any pins relative to V _{SS}	V _{IN} , V _{OUT}	-0.4V ~ 1.975	V	1
DRAM Storage temperature	T _{STG}	-55 ~ 100	°C	1,2
DRAM Operation temperature (Standard Product)	T _{case}	0 ~ 95	°C	2,4,6
DRAM Operation temperature (Industrial Temperature Product)	T _{case}	-40 ~ 95	°C	2,5,6

- Notes:
- Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
 - Storage Temperature or DRAM operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC51-2 standard.
 - V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REF} must not be greater than 0.6 x V_{DDQ}, when V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.
 - The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-95 °C under all operating conditions.
 - The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between -40-95 °C under all operating conditions.
 - Some applications require operation of the Extended Temperature Range between 85 °C and 95 °C case temperature. Full Specifications are guaranteed in this range but the following additional conditions apply a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us. b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

Table 11 - DC Electrical Characteristics and Operating Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ	Max		
Supply voltage	V _{DD}	1.283	1.35	1.45	V	1,2
I/O supply voltage	V _{DDQ}				V	1,2
Supply voltage	V _{DD}	1.425	1.5	1.575	V	1,2,3
I/O supply voltage	V _{DDQ}				V	1,2,3

- Notes:
- V_{DD} and V_{DDQ} must track one another. V_{DDQ} must be less than or equal to V_{DD}. V_{SS} = V_{SSQ}.
 - V_{DD} and V_{DDQ} may include AC noise of +/-50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. V_{DD} and V_{DDQ} must be at same level for valid AC timing parameters.
 - Module is backward-compatible with 1.5V operation.

Table 12 - DC Electrical Characteristics and Input Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ	Max		
V _{IN} low; DC/commands/address buses (1.35V)	V _{IL}	V _{SS}	-	-0.090	V	
V _{IN} low; DC/commands/address buses (1.5V)	V _{IL}	V _{SS}	-	-0.100	V	
V _{IN} high; DC/commands/address buses (1.35V)	V _{IH}	0.090	-	V _{DD}	V	
V _{IN} high; DC/commands/address buses (1.5V)	V _{IH}	0.100	-	V _{DD}	V	
Input reference voltage; command/address bus	V _{REFCA(DC)}	0.49* V _{DD}	0.50* V _{DD}	0.51* V _{DD}	V	1,2
I/O reference voltage DQ bus	V _{REFDQ(DC)}	0.49* V _{DD}	0.50* V _{DD}	0.51* V _{DD}	V	2,3
Command/address termination voltage (system level, not direct DRAM input)	V _{TT}	-	0.50* V _{DDQ}	-	V	4

Notes:

- 1 V_{REFCA(DC)} is expected to be approximately 0.5 × V_{DD} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFCA} may not exceed ±1% × V_{DD} around the V_{REFCA(DC)} value. Peak-to-peak AC noise on V_{REFCA} should not exceed ±2% of V_{REFCA(DC)}.
- 2 DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20 MHz in frequency.
- 3 V_{REFDQ(DC)} is expected to be approximately 0.5 × V_{DD} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFDQ} may not exceed ±1% × V_{DD} around the V_{REFDQ(DC)} value. Peak-to-peak AC noise on V_{REFDQ} should not exceed ±2% of V_{REFDQ(DC)}.
- 4 V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors. MIN and MAX values are system-dependent.

Table 13 - Input Switching Conditions

Parameter / Condition	Symbol	Value		Units
		1.35V	1.5V	
Command and Address				
Input high AC voltage: Logic 1 @ 175mV	$V_{IH(AC175)min}$	-	175	mV
Input high AC voltage: Logic 1 @ 160mV	$V_{IH(AC160)min}$	160	-	mV
Input high AC voltage: Logic 1 @ 150mV	$V_{IH(AC150)min}$	-	150	mV
Input high AC voltage: Logic 1 @ 135mV	$V_{IH(AC135)min}$	135	-	mV
Input high DC voltage: Logic 1 @ 100mV	$V_{IH(DC100)min}$	-	100	mV
Input high DC voltage: Logic 1 @ 90mV	$V_{IH(DC90)min}$	90	-	mV
Input low DC voltage: Logic 0 @ -90mV	$V_{IL(DC90)max}$	-90	-	mV
Input low DC voltage: Logic 0 @ -100mV	$V_{IL(DC100)max}$	-	-100	mV
Input low AC voltage: Logic 0 @ -135mV	$V_{IL(AC135)max}$	-135	-	mV
Input low AC voltage: Logic 0 @ -150mV	$V_{IL(AC150)max}$	-	-150	mV
Input low AC voltage: Logic 0 @ -160mV	$V_{IL(AC160)max}$	-160	-	mV
Input low AC voltage: Logic 0 @ -175mV	$V_{IL(AC175)max}$	-	-175	mV

Parameter / Condition	Symbol	Value		Units
		1.35V	1.5V	
DQ and DM				
Input high AC voltage: Logic 1	$V_{IH(AC150)min}$	-	150	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}$	135	-	mV
Input high DC voltage: Logic 1	$V_{IH(DC100)min}$	-	100	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	-	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)max}$	-90	-	mV
Input low DC voltage: Logic 0	$V_{IL(DC100)max}$	-	-100	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)max}$	-135	-	mV
Input low AC voltage: Logic 0	$V_{IL(AC150)max}$	-	-150	mV

- Notes:
1. All voltages are referenced to V_{REF} . V_{REF} is V_{REFCA} for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. V_{REF} is V_{REFDQ} for DQ and DM inputs.
 2. Input setup timing parameters (t_{IS} and t_{DS}) are referenced at $V_{IL(AC)}/V_{IH(AC)}$, not $V_{REF(DC)}$.
 3. Input hold timing parameters (t_{IH} and t_{DH}) are referenced at $V_{IL(DC)}/V_{IH(DC)}$, not $V_{REF(DC)}$.
 4. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).

Table 14 - Differential Input Operating Conditions (CK, /CK and DQS, /DQS)

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Differential input voltage logic high – slew (1.35V)	$V_{IH,diff}$	+180	-	mV	1
Differential input voltage logic high – slew (1.5V)	$V_{IH,diff}$	+200	-	mV	1
Differential input voltage logic low – slew (1.35V)	$V_{IL,diff}$	-	-180	mV	1
Differential input voltage logic low – slew (1.5V)	$V_{IL,diff}$	-	-200	mV	1
Differential input voltage logic high	$V_{IH,diff(AC)}$	$2 * (V_{IH(AC)} - V_{REF})$	-	mV	2
Differential input voltage logic low	$V_{IL,diff(AC)}$	-	$2 * (V_{IL(AC)} - V_{REF})$	mV	3
Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK, CK (1.35V)	V_{IX}	-150	150	mV	4
Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK, CK (1.5V)	V_{IX}	-150	150	mV	5
		-175	175		
Differential Input Cross Point Voltage relative to $V_{DD}/2$ for DQS, DQS (1.35V)	V_{IX}	-150	150	mV	
Differential Input Cross Point Voltage relative to $V_{DD}/2$ for DQS, DQS (1.5V)	V_{IX}	-150	150	mV	

Notes:

- 1 Defines slew rate reference points, relative to input crossing voltages.
- 2 Minimum DC limit is relative to single-ended signals; overshoot specifications are applicable.
- 3 Maximum DC limit is relative to single-ended signals; undershoot specifications are applicable.
- 4 The relation between V_{IX} Min/Max and V_{SEL}/V_{SEH} should satisfy following:
 $(V_{DD}/2) + V_{IX(min)} - V_{SEL} \geq 25mV;$
 $V_{SEH} - ((V_{DD}/2) + V_{IX(max)}) \geq 25mV;$
- 5 Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and /CK are monotonic with a single-ended swing V_{SEL}/V_{SEH} of at least $V_{DD}/2 \pm 250mV$, and when the differential slew rate of CK-/CK is larger than 3V/ns.

Table 15 - Single-Ended Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{REF} - 0.1 * V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.1 * V_{DDQ}$ (1.35V)	SRQ _{se}	1.75	5	V/ns	1,2,3
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{REF} - 0.1 * V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.1 * V_{DDQ}$ (1.5V)	SRQ _{se}	2.5	5	V/ns	1,2,3
Single-ended high level for strobes	V _{SEH}	$V_{DD}/2 + 175$	-	mV	2
Single-ended high level for CK, /CK		$V_{DD}/2 + 175$	-	mV	2
Single-ended low level for strobes	V _{SEL}	-	$V_{DD}/2 - 175$	mV	3
Single-ended low level for CK, /CK		-	$V_{DD}/2 - 175$	mV	3
Single-ended DC high-level output voltage	V _{OH(DC)}	$0.8 * V_{DDQ}$		V	1
Single-ended DC mid-level output voltage	V _{OM(DC)}	$0.5 * V_{DDQ}$		V	1
Single-ended DC low-level output voltage	V _{OL(DC)}	$0.2 * V_{DDQ}$		V	1
Single-ended AC high-level output voltage	V _{OH(AC)}	$V_{TT} + 0.1 * V_{DDQ}$		V	1,2
Single-ended AC low-level output voltage	V _{OL(AC)}	$V_{TT} - 0.1 * V_{DDQ}$		V	1,2
Test load for AC timing and output slew rates	Output to V_{TT} ($V_{DDQ}/2$) via 25Ω resistor				

Notes:

1. RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$, $V_{SSQ} = V_{SS}$).
2. $V_{TT} = V_{DDQ}/2$.
3. The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or all switching the opposite direction. For all other DQ signal switching combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.

Table 16 - Differential Output Driver Characteristics

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)} = -0.2 * V_{DDQ}$ and $V_{OH,diff(AC)} = +0.2 * V_{DDQ}$ (1.35V)	SRQ _{diff}	3.5	12	V/ns	1
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)} = -0.2 * V_{DDQ}$ and $V_{OH,diff(AC)} = +0.2 * V_{DDQ}$ (1.5V)	SRQ _{diff}	5	10	V/ns	1
Differential high-level output voltage	V _{OH,diff(AC)}	$+0.2 * V_{DDQ}$		V	1
Differential low-level output voltage	V _{OL,diff(AC)}	$-0.2 * V_{DDQ}$		V	1
Test load for AC timing and output slew rates	Output to V_{TT} ($V_{DDQ}/2$) via 25Ω resistor				

Notes:

1. RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$, $V_{SSQ} = V_{SS}$).
2. $V_{REF} = V_{DDQ}/2$; slew rate @ 5V/ns, interpolate for faster slew rate.

For part number IMM2G72D3LRVQ8AG-C125(I)

Table 17 - IDD Specifications with Conditions and Operation Current

Parameter / Condition	Symbol	Current	Units	Notes
Operating current 0; One bank ACTIVATE-to-PRECHARGE	I _{DD0}	954	mA	1, 2
Operating current 1; One bank ACTIVATE-to-READ-to-PRECHARGE	I _{DD1}	1089	mA	1, 2
Precharge power-down current (Slow Exit)	I _{DD2P0}	468	mA	1, 3
Precharge standby ODT current	I _{DD2NT}	1170	mA	1, 3
Active power-down current	I _{DD3P}	810	mA	1, 3
Active standby current	I _{DD3N}	1260	mA	1, 3
Burst read operating current	I _{DD4R}	1539	mA	1, 2
Burst write operating current	I _{DD4W}	1584	mA	1, 2
Refresh current	I _{DD5B}	2664	mA	1, 2
Self refresh temperature current: MAX T _c = 85°C	I _{DD6}	540	mA	1, 3
Self refresh temperature current (SRT-enabled): MAX T _c = 95°C	I _{DD6ET}	720	mA	1, 3
All banks interleaved read current	I _{DD7}	2304	mA	1, 2
RESET Low Current	I _{DD8}	540	mA	1, 3

Notes:

- ¹ Value shown for DDR3 SDRAM only and are computed from values specified in the 8Gbit component data sheet.
- ² One module rank in the active IDD, the other rank in IDD2P0.
- ³ All ranks in this IDD conditions.

For part number IMM2G72D3LRVQ8AG-C125(I)

Table 18 - AC Timing Parameter and Operating Conditions

Parameter / Condition		Symbol	Min	Max	Units
Clock Timing					
Clock period average: DLL disable mode	T _c = 0°C to 85°C	t ^{CK} (DLL_DIS)	8	7800	ns
	T _c => 85°C to 95°C		8	3900	
Clock periods average: DLL enable mode (CL = 11, CWL = 8)		t ^{CK} (AVG)	1.25	<1.5	ns
Clock periods average: DLL enable mode (CL = 9, CWL = 7)		t ^{CK} (AVG)	1.5	<1.875	ns
High pulse width average		t ^{CH} (AVG)	0.47	0.53	t ^{CK}
Low pulse width average		t ^{CL} (AVG)	0.47	0.53	t ^{CK}
Clock period jitter	DLL locked	t ^{JITper}	-70	70	ps
	DLL locking	t ^{JITper,lck}	-60	60	ps
Clock absolute period		t ^{CK} (ABS)	t ^{CK} (AVG) MIN + t ^{JITper} MIN	t ^{CK} (AVG) MAX + t ^{JITper} MAX	ps
Clock absolute high pulse width		t ^{CH} (ABS)	0.43	-	t ^{CK} (AVG)
Clock absolute low pulse width		t ^{CL} (ABS)	0.43	-	t ^{CK} (AVG)
Cycle-to-cycle jitter	DLL locked	t ^{JITcc}	-	140	ps
	DLL locking	t ^{JITcc,lck}	-	120	ps
Cumulative error across	2 cycles	t ^{ERR2per}	-103	103	ps
	3 cycles	t ^{ERR3per}	-122	122	ps
	4 cycles	t ^{ERR4per}	-136	136	ps
	5 cycles	t ^{ERR5per}	-147	147	ps
	6 cycles	t ^{ERR6per}	-155	155	ps
	7 cycles	t ^{ERR7per}	-163	163	ps
	8 cycles	t ^{ERR8per}	-169	169	ps
	9 cycles	t ^{ERR9per}	-175	175	ps
	10 cycles	t ^{ERR10per}	-180	180	ps
	11 cycles	t ^{ERR11per}	-184	184	ps
	12 cycles	t ^{ERR12per}	-188	188	ps
	n = 14,...49, 50 cycles	t ^{ERRnper}	(1+0.68ln[n]) * t ^{JITper} MIN	(1+0.68ln[n]) * t ^{JITper} Max	ps
DQ Input Timing					
Data setup time to DQS, /DQS (1.35V)	Base (specification)	t ^{DS} (AC135)	25	-	ps
Data setup time to DQS, /DQS (1.5V)	Base (specification)	t ^{DS} (AC150)	10	-	ps
Data hold time from DQS, /DQS (1.35V)	Base (specification)	t ^{DH} (DC90)	55	-	ps
Data hold time from DQS, /DQS (1.5V)	Base (specification)	t ^{DH} (DC100)	45	-	ps
Minimum data pulse width		t ^{DIPW}	360	-	ps
DQ Output Timing					
DQS, /DQS to DQ skew, per access		t ^{DQSQ}	-	100	ps
DQ output hold time from DQS, /DQS		t ^{QH}	0.38	-	t ^{CK} (AVG)
DQ Low-Z time from CK, /CK		t ^{LZDQ}	-450	225	ps
DQ High-Z time from CK, /CK		t ^{HZDQ}	-	225	ps
DQ Strobe Input Timing					
DQS, /DQS rising to CK, /CK rising		t ^{DQSS}	-0.27	0.27	t ^{CK}
DQS, /DQS differential input low pulse width		t ^{DQSL}	0.45	0.55	t ^{CK}

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Parameter / Condition		Symbol	Min	Max	Units
DQS, /DQS falling setup to CK, /CK rising		^t DSS	0.18	-	^t CK
DQS, /DQS falling hold from CK, /CK rising		^t DSH	0.18	-	^t CK
DQS, /DQS differential input high pulse width		^t DQSH	0.45	0.55	^t CK
DQS, /DQS differential WRITE preamble		^t WPRE	0.9	-	^t CK
DQS, /DQS differential WRITE postamble		^t WPST	0.3	-	^t CK
DQ Strobe Output Timing					
DQS, /DQS rising to/from CK, /CK		^t DQSCK	-225	225	ps
DQS, /DQS differential output high time		^t QSH	0.40	-	^t CK
DQS, /DQS differential output low time		^t QSL	0.40	-	^t CK
DQS, /DQS Low-Z time (RL-1)		^t LZDQS	-450	225	ps
DQS, /DQS High-Z time (RL+BL/2)		^t HZDQS	-	225	ps
DQS, /DQS differential READ preamble		^t RPRE	0.9	greater of ^t LZ(DQS) (MIN), ^t DQSCK (MAX)	^t CK
DQS, /DQS differential READ postamble		^t RPST	0.3	greater of ^t DQSCK (MIN) + ^t QSH (MIN), ^t HZ(DQS) (MAX)	^t CK
Command and Address Timing					
DLL locking time		^t DLLK	512	-	^t CK
CTRL, CMD, ADDR setup to CK, /CK (1.35V)	Base (specification)	^t IS (AC160)	60	-	ps
CTRL, CMD, ADDR setup to CK, /CK (1.5V)	Base (specification)	^t IS (AC175)	45	-	ps
CTRL, CMD, ADDR setup to CK, /CK (1.35V)	Base (specification)	^t IS (AC135)	185	-	ps
CTRL, CMD, ADDR setup to CK, /CK (1.5V)	Base (specification)	^t IS (AC150)	170	-	ps
CTRL, CMD, ADDR hold from CK, /CK (1.35V)	Base (specification)	^t IH (DC90)	130	-	ps
CTRL, CMD, ADDR hold from CK, /CK (1.5V)	Base (specification)	^t IH (DC100)	120	-	ps
Minimum CTRL, CMD, ADDR pulse width		^t IPW	560	-	ps
ACTIVATE to internal READ or WRITE delay		^t RCD	13.125	-	ns
PRECHARGE command period		^t RP	13.125	-	ns
ACTIVATE-to-PRECHARGE command period		^t RAS	35	9 * ^t REFI	ns
ACTIVATE-to-ACTIVATE command period		^t RC	48.125	-	ns
ACTIVATE-to-ACTIVATE minimum period		^t RRD	greater of 4 ^t CK or 6ns	-	^t CK
Four ACTIVATE windows (2KB page size)		^t FAW	30	-	ns
Write recovery time		^t WR	15	-	ns
Delay from start of internal WRITE transaction to internal READ command		^t WTR	greater of 4 ^t CK or 7.5ns	-	^t CK
READ-to-PRECHARGE time		^t RTP	greater of 4 ^t CK or 7.5ns	-	^t CK
/CAS-to-/CAS command delay		^t CCD	4	-	^t CK
Auto precharge write recovery + precharge time		^t DAL	WR + ^t RP/ ^t CK (AVG)	-	^t CK
MODE REGISTER SET command cycle time		^t MRD	4	-	^t CK
MODE REGISTER SET command update delay		^t MOD	greater of 12 ^t CK or 15ns	-	^t CK
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		^t MPPRR	1	-	^t CK

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Parameter / Condition		Symbol	Min	Max	Units
Calibration Timing					
ZQCL command: Long calibration time	POWER-UP and RESET operation	$t'ZQinit$	greater of 512 $t'CK$ or 640ns	-	$t'CK$
	Normal operation	$t'ZQoper$	greater of 256 $t'CK$ or 320ns	-	$t'CK$
ZQCS command: Short calibration time		$t'ZQcs$	greater of 64 $t'CK$ or 80ns	-	$t'CK$
Initialization and Reset Timing					
Exit reset from CKE HIGH to valid command		$t'XPR$	greater of 5 $t'CK$ or $t'RFC(min)+10ns$	-	$t'CK$
Refresh Timing					
REFRESH-to-ACTIVATE or REFRESH command period		$t'RFC$	260	-	ns
Maximum refresh period	$T_c \leq 85^\circ C$	-	64 (1X)	-	ms
	$T_c > 85^\circ C$	-	32 (2X)	-	
Maximum average periodic refresh	$T_c \leq 85^\circ C$	$t'REFI$	7.8 (64ms/8192)	-	us
	$T_c > 85^\circ C$		3.9 (32ms/8192)	-	
Self Refresh Timing					
Exit self refresh to commands not requiring a locked DLL		$t'XS$	greater of 5 $t'CK$ or $t'RFC+10ns$	-	$t'CK$
Exit self refresh to commands requiring a locked DLL		$t'XSDLL$	$t'DLLK (MIN)$	-	$t'CK$
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		$t'CKESR$	$t'CKE (MIN) + t'CK$	-	$t'CK$
Valid clocks after self refresh entry or power down entry		$t'CKSRE$	greater of 5 $t'CK$ or 10ns	-	$t'CK$
Valid clocks before self refresh exit, power-down exit, or reset exit		$t'CKSRX$	greater of 5 $t'CK$ or 10ns	-	$t'CK$
Power-Down Timing					
CKE MIN pulse width		$t'CKE (MIN)$	greater of 3 $t'CK$ or 5ns	-	$t'CK$
Command pass disable delay		$t'CPDED$	1	-	$t'CK$
Power-down entry to power exit timing		$t'PD$	$t'CKE (MIN)$	9 * $t'REFI$	$t'CK$
Power-Down Entry Minimum Timing					
ACTIVATE command to power-down entry		$t'ACTPDEN$	1	-	$t'CK$
PRECHARGE/PRECHARGE ALL command to power-down entry		$t'PRPDEN$	1	-	$t'CK$
REFRESH command to power-down entry		$t'REFPDEN$	1	-	$t'CK$
MRS command to power-down entry		$t'MRSPDEN$	MIN = $t'MOD (MIN)$		$t'CK$
READ/READ with auto precharge command to power-down entry		$t'RDPDEN$	MIN = $RL + 4 + 1$		$t'CK$
WRITE command to power-down entry	BL8 (OTF, MRS)	$t'WRPDEN$	MIN = $WL + 4 + t'WR/t'CK (AVG)$		$t'CK$
	BC4MRS		MIN = $WL + 2 + t'WR/t'CK (AVG)$		
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS)	$t'WRAPDEN$	MIN = $WL + 4 + t'WR + 1$		$t'CK$
	BC4MRS		MIN = $WL + 2 + t'WR + 1$		
Power-Down Exit Timing					
DLL on, any valid command, or DLL off to commands not requiring locked DLL		$t'XP$	greater of 3 $t'CK$ or 6ns	-	$t'CK$
Precharge power-down with DLL off to commands requiring a locked DLL		$t'XPDLL$	greater of 10 $t'CK$ or 24ns	--	$t'CK$
ODT Timing					
R_{TT} turn-on from ODTL on reference		$t'AON$	-225	225	ps
R_{TT} turn-off from ODTL off reference		$t'AOF$	0.3	0.7	$t'CK (AVG)$

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Parameter / Condition	Symbol	Min	Max	Units
Asynchronous R _{TT} turn-on delay (power-down with DLL off)	t'AONPD	2	8.5	ns
Asynchronous R _{TT} turn-off delay (power-down with DLL off)	t'AOPFD	2	8.5	ns
ODT high time without write command or with write command and BC4	ODTH4	4	-	t'CK
ODT high time with Write command and BL8	ODTH8	6	-	t'CK
Dynamic ODT Timing				
R _{TT} dynamic change skew	t'ADC	0.3	0.7	t'CK (AVG)
Write Leveling Timing				
First DQS, /DQS rising edge	t'WLMRD	40	-	t'CK
DQS, /DQS delay	t'WLDQSEN	25	-	t'CK
Write leveling setup from rising CK, /CK crossing to rising DQS, /DQS crossing	t'WLS	165	-	ps
Write leveling hold from rising DQS, /DQS crossing to rising CK, /CK crossing	t'WLH	165	-	ps
Write leveling output delay	t'WLO	0	7.5	ns
Write leveling output error	t'WLOE	0	2	ns

For part number IMM2G72D3LRVQ8AG-C125(I)

Table 19 - SPD Information

Byte NO.	Description	Note	Hex
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	176 / 256 / 0-116	92
1	SPD Revision	1.2	12
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte / Module Type	72bit Registered DIMM	01
4	SDRAM Density and Banks	4Gb 8banks	04
5	SDRAM Addressing	Row 16 / Col 10	21
6	Module Nominal Voltage, V _{DD}	1.35V/1.5V	02
7	Module Organization	4Rank , x8	19
8	Module Memory Bus Width	ECC, 72bit	0B
9	Fine Timebase (FTB) Dividend and Divisor	2.5ps	52
10	Medium Timebase (MTB) Dividend	1/8 (0.125ns)	01
11	Medium Timebase (MTB) Divisor	1/8 (0.125ns)	08
12	SDRAM Minimum Cycle Time (tCKmin)	1.25ns	0A
13	Reserved	-	00
14	CAS Latencies Supported, Least Significant Byte	5, 6, 7, 8, 9, 10, 11	FE
15	CAS Latencies Supported, Most Significant Byte	-	00
16	Minimum CAS Latency Time (tAamin)	13.125ns	69
17	Minimum Write Recovery Time (tWRmin)	15ns	78
18	Minimum /RAS to /CAS Delay Time (tRCDmin)	13.125ns	69
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	6ns	30
20	Minimum Row Precharge Time (tRPmin)	13.125ns	69
21	Upper Nibbles for tRAS and tRC	-	11
22	Minimum Active to Precharge Time (tRASmin), LSB	35ns	18
23	Minimum Active to Active/Refresh Time (tRCmin), LSB	48.125ns	81
24	Minimum Refresh Recovery Time (tRFCmin), LSB	260ns	20
25	Minimum Refresh Recovery Time (tRFCmin), MSB	260ns	08
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	7.5ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns	3C
28	Upper Nibble for tFAW	30ns	00
29	Minimum Four Activate Window Delay Time (tFAWmin), LSB	30ns	F0
30	SDRAM Optional Features	DLL off Mode, RZQ/6, RZQ/7	83
31	SDRAM Thermal and Refresh Options	0-95oC Op. Temp. w/2x refresh	05
32	Module Thermal Sensor	With TS	80
33	SDRAM Device Type	Non-Standard SDRAM	A1

Byte NO.	Description	Note	Hex
34-59	Reserved, General Section	-	00
60	Module Nominal Height	18< Height <= 19	04
61	Module Maximum Thickness	1< Tf <=2 (mm); 1< Tb <=2 (mm)	11
62	Reference Raw Card Used	Raw card V0	11
63	Address Mapping from Edge Connector to DRAM	1 Row of DRAM / 1 Register Used	05
64	Heat Spreader Solution	Without HS	00
65	Register vendor ID code (LSB)	-	00
66	Register vendor ID code (MSB)	-	00
67	Register Revision Number	-	FF
68	Register Type	SSTE32882	00
69	Register Control Word Function (RC0/RC1)	-	00
70	Register Control Word Function (RC2/RC3)	Moderate Drive	50
71	Register Control Word Function (RC4/RC5)	Moderate Drive	55
72	Register Control Word Function (RC6/RC7)	-	00
73	Register Control Word Function (RC8/RC9)	-	00
74	Register Control Word Function (RC10/RC11)	-	00
75	Register Control Word Function (RC12/RC13)	-	00
76	Register Control Word Function (RC14/RC15)	-	00
77-116	Reserved	-	00
117-118	Module ID: Module Manufacturer's JEDEC ID Code	Reserved	Reserved
119	Module ID: Module Manufacturing Location	Reserved	Reserved
120-121	Module ID: Module Manufacturing Date	Reserved	Reserved
122-125	Module ID: Module Serial Number	Reserved	Reserved
126-127	Cyclical Redundancy Code	-	14 52
128-145	Module Part Number	Reserved	Reserved
146-147	Module Revision Code	Reserved	Reserved
148-149	DRAM Manufacturer's JEDEC ID Code	Reserved	Reserved
150-175	Manufacturer's Specific Data	Reserved	Reserved
176-255	Open For Customer Use	Reserved	Reserved

Revision History

Revision	Descriptions	Release Date
1.0	Initial release	Mar, 2018

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