PRELIMINARY

IM4G16L4JCB
4Gbit LPDDR4x SDRAM
8 Bank x 32Mbit x 16 x 1 Channel

	046
	LPDDR4-4266
Clock Cycle Time (tCK)	0.468ns
System Frequency ($f_{CK(MAX)}$)	2133MHz

Specification

- Density: 4Gbits
- Organization: 8 Bank x 32Mbit x 16 x 1 Channel
- Data rate: 4266Mbps
- Double-Data Rate Architecture
- Bi-directional Data Strobe (DQS)
- Differential Clock Input (CK_t, CK_c)
- Differential Data Strobe (DQS_t, DQS_c)
- Command and Address entered positive CK edge; Data and Data Mask referenced to both edges of DQS
- DMI Pin
  - DBI (Data Bus Inversion) during normal Read and Write
  - Counting # of DQ's 1 for Masked Write when DBI on
  - DM (Data Mask) for Masked Write when DBI off
- 8 Internal Bank for each Channel
- Burst Length: 16, 32(OTF)
- Burst Type: Sequential
- Auto Precharge option for each Burst Access
- Configurable Drive Strength
- Refresh and Self Refresh mode
- Partial Array Self Refresh and Temperature Compensated Self Refresh
- Write Leveling
- CA Calibration
- Internal V_{REF} and V_{REF} Training
- FIFO based Write/Read Training
- MPC (Multi-Purpose Command)
- LVSTLE (Low Voltage Swing Terminated Logic Extension) I/O
- Power Supply:
  - V_{DD1} = 1.8V
  - V_{DD2} = 1.1V
  - V_{DDQ} = 0.6V
- V_{SSQ} Termination
- Edge align Data Output; Center algin for Write Training Data Input
- Refresh Rate: 3.9µs

Option

Option	Marking
• Configuration	
- 8 Bank x 32Mbit x 16 x 1Ch (4Gbit)	4G16
• Package	
- 200-Ball FBGA, Single Rank	B
• RoHS Compliance	
- RoHS Compliance	G
- Leaded	[Blank]
• Speed	
- LPDDR4-4266 (0.468ns)	046
• Temperature (T_{CASE})	
- Commercial Temperature (-25℃ to 85℃)	[Blank]
- Industrial Temperature (-40℃ to 95℃)	I
• Automotive Grade	
- Non-Automotive Grade	[Blank]

Example Part Number: IM4G16L4JCBG-046I

Part Number Information

IM 4G 16 L4 J C B G - 046 (I) ()

Intelligent Memory

DRAM Density
4G = 4Gbit

DRAM I/O width
16 = x16

Memory Type
L4 = LPDDR4 & LPDDR4x

Voltage
J = 1.8V/1.1V; V_{DDQ} =0.6V (LPDDR4x)

DRAM Revision
C = Revision C

Automotive Grade
Blank = Non-Automotive Grade

Temperature
Blank = Commercial Temp -25°C to +85°C T_{CASE}
I = Industrial Temp -40°C to +95°C T_{CASE}

Speed
046 = LPDDR4-4266

RoHS Compliance
G = RoHS Compliance
Blank = Leaded

Package
B = 200-Ball FBGA, Single Rank

LPDDR4x SDRAM Addressing

Configuration		**LPDDR4x**
Memory Density		4Gbit
Configuration		8 Bank x 32Mb x 16 x 1 Channel
Number of Channel		1
Channel Density		4Gbit
Total Density (per Channel)		4Gbit
Number of Bank (per Channel)		8
Number of Row (per Channel)		32,768
Number of Column (Fetch Boundaries)		64
Array Pre-Fetch (bit, per Channel)		256
Page Size (Byte)		2,048
Burst Starting Address Boundary		64bit
Bank Address		BA0 ~ BA2
x16	Row Address[2]	R0 ~ R14
	Column Address[1,2]	C0 ~ C9

Note:
1. The lower two column addresses (C0-C1) are assumed to be “zero” and are not transmitted on the CA bus.
2. Row and Column address values on the CA bus that are not used for a particular density be at valid logic level.

Pin Configuration

200-Ball FBGA (x16 configuration)

0.80mm Pitch (columns); 0.65mm Pitch (rows)

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	V_{SS}	V_{DD2}	ZQ0			NC	V_{DD2}	V_{SS}	DNU	DNU
B	DNU	DQ0_A	V_{DDQ}	DQ7_A	V_{DDQ}			V_{DDQ}	DQ15_A	V_{DDQ}	DQ8_A	DNU
C	V_{SS}	DQ1_A	DMI0_A	DQ6_A	V_{SS}			V_{SS}	DQ14_A	DM1_A	DQ9_A	V_{SS}
D	V_{DDQ}	V_{SS}	DQS0_t_A	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	DQS1_t_A	V_{SS}	V_{DDQ}
E	V_{SS}	DQ2_A	DQS0_c_A	DQ5_A	V_{SS}			V_{SS}	DQ13_A	DQS1_c_A	DQ10_A	V_{SS}
F	V_{DD1}	DQ3_A	V_{DDQ}	DQ4_A	V_{DD2}			V_{DD2}	DQ12_A	V_{DDQ}	DQ11_A	V_{DD1}
G	V_{SS}	ODT_CA_A[1]	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	NC	V_{SS}
H	V_{DD2}	CA0_A	NC	CS0_A	V_{DD2}			V_{DD2}	CA2_A	CA3_A	CA4_A	V_{DD2}
J	V_{SS}	CA1_A	V_{SS}	CKE0_A	NC			CK_t_A	CK_c_A	V_{SS}	CA5_A	V_{SS}
K	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	NC			NC	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
L												
M												
N	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	NC			NC	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
P	V_{SS}	NC	V_{SS}	NC	NC			NC	NC	V_{SS}	NC	V_{SS}
R	V_{DD2}	NC	NC	NC	V_{DD2}			V_{DD2}	NC	NC	NC	V_{DD2}
T	V_{SS}	NC	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	RESET_n	V_{SS}
U	V_{DD1}	NC	V_{DDQ}	NC	V_{DD2}			V_{DD2}	NC	V_{DDQ}	NC	V_{DD1}
V	V_{SS}	NC	NC	NC	V_{SS}			V_{SS}	NC	NC	NC	V_{SS}
W	V_{DDQ}	V_{SS}	NC	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	NC	V_{SS}	V_{DDQ}
Y	V_{SS}	NC	NC	NC	V_{SS}			V_{SS}	NC	NC	NC	V_{SS}
AA	DNU	NC	V_{DDQ}	NC	V_{DDQ}			V_{DDQ}	NC	V_{DDQ}	NC	DNU
AB	DNU	DNU	V_{SS}	V_{DD2}	V_{SS}			V_{SS}	V_{DD2}	V_{SS}	DNU	DNU

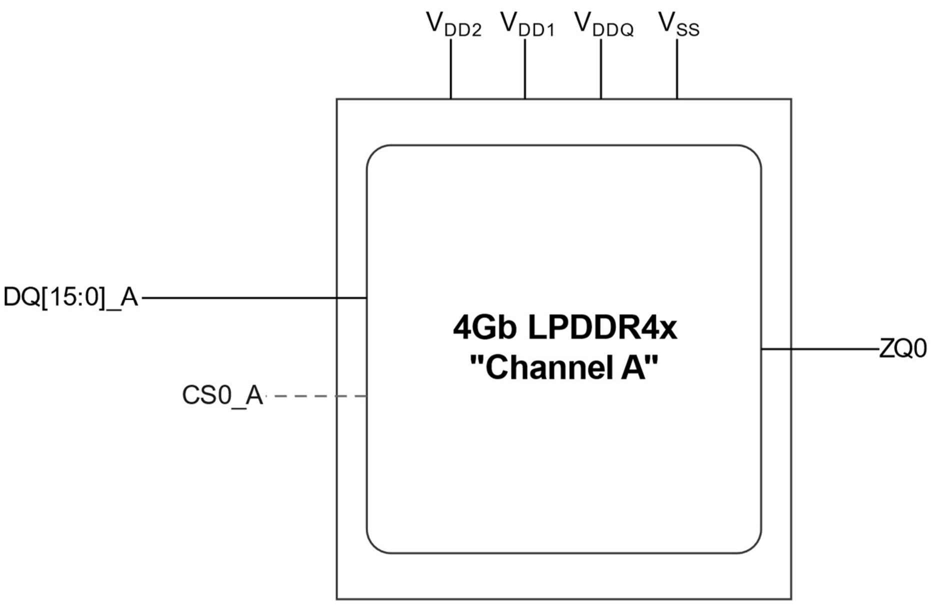
Note:

1. ODT_CA_[x] balls are wired to ODT_CA_[x] pads of Rank 0 DRAM die. ODT_CA_[x] pads for other ranks (if present) are disabled in the package
2. In case ODT function is not used, ODT pin should be considered as NC.
3. ODT will be connected to rank 0. The ODT input to rank 1 (if rank 2 is present) will be connected to ground in the package.

Signal Pin Description

Pin	Type	Function
CK_t_A, CK_c_A	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK.
CKE0_A	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code.
CS0_A	Input	**Chip Select:** CS is part of the command code.
CA[5:0]_A	Input	**Command/Address Input:** CA signals provide the command and address inputs according to the Command Truth Table.
ODT_CA_A	Input	**CA ODT Control:** The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins.
DQ[15:0]_A	I/O	**Data Input/Output:** Bi-direction data bus
DQS[1:0]_t_A, DQS[1:0]_c_A	I/O	**Data Strobe:** DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair.
DMI[1:0]_A	Input	**Data Mask Inversion:** DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting.
ZQ0	Reference	**Calibration Reference:** Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240ohm ± 1% resistor.
RESET_n	Input	**RESET:** When asserted Low, the RESET_n signal resets all channels of the die. There is one RESET_n pad per die.
V_{DDQ}, V_{DD1}, V_{DD2}	Supply	**Power Supplies:** Isolated on the die for improved noise immunity.
V_{SS}, V_{SSQ}	GND	**Ground Reference:** Power supply ground reference.
NC	-	**No Connect**

Function Block Diagram

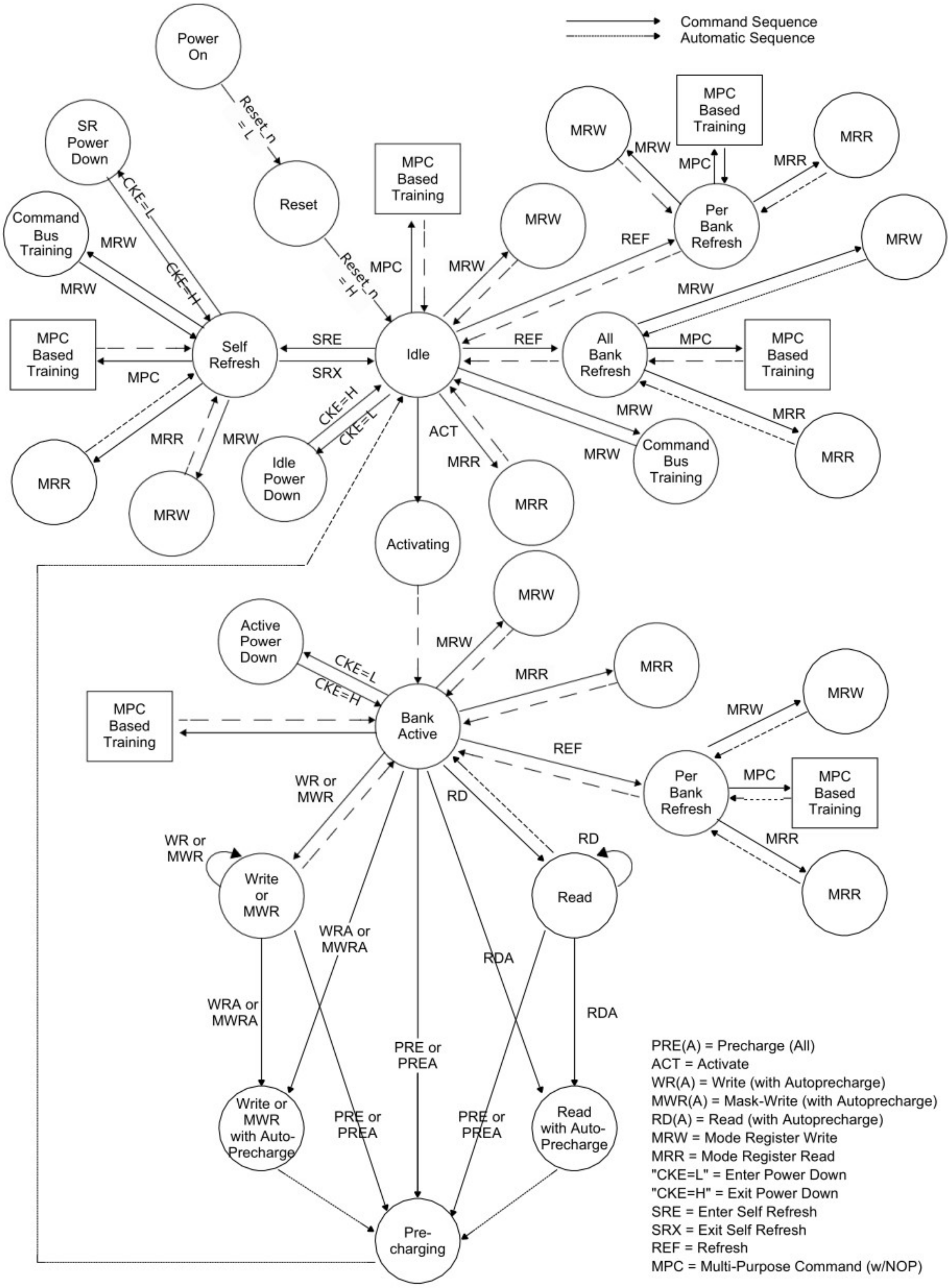


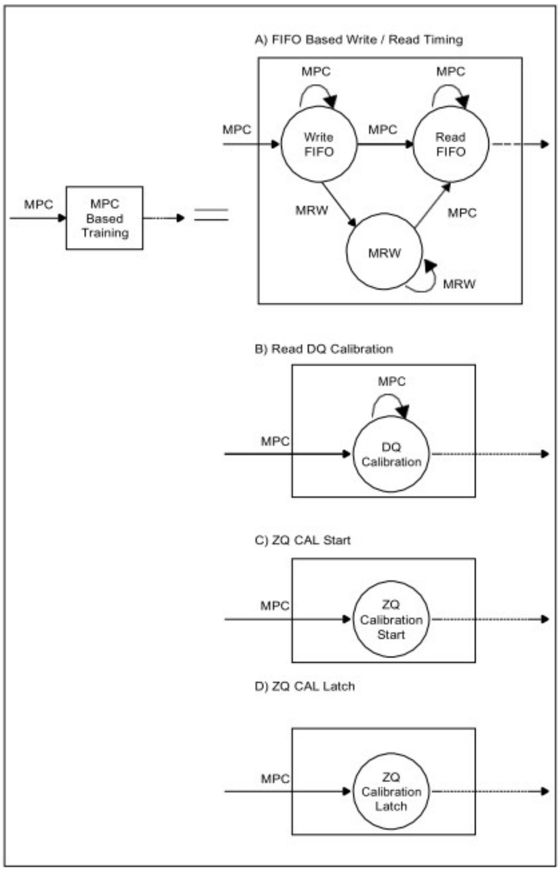
Simplified State Diagram

LPDDR4 SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram; they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see Section “Command Definition and Timing Diagram”.





Note:

1. From the Self-Refresh state the device can enter Power-Down, MRR, MRW, or MPC states. See the section on Self-Refresh for more information.
2. In IDLE state, all banks are precharged.
3. In the case of a MRW command to enter a training mode, the state machine will not automatically return to the IDLE state at the conclusion of training. See the applicable training section for more information.
4. In the case of a MPC command to enter a training mode, the state machine may not automatically return to the IDLE state at the conclusion of training. See the applicable training section for more information.
5. This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.
6. States that have an “automatic return” and can be accessed from more than one prior state (Ex. MRW from either Idle or Active states) will return to the state from when they were initiated (Ex. MRW from Idle will return to Idle).
7. The RESET_n pin can be asserted from any state, and will cause the SDRAM to go to the Reset State. The diagram shows RESET applied from the Power-On as an example, but the Diagram should not be construed as a restriction on RESET_n.

Power-up Initialization and Power-off Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as below Table.

Item	MRS	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00_B	FSP-OP/WR[0] are enabled
WLS	MR2 OP[6]	0_B	Write Latency Set 0 is selected
WL	MR2 OP[5:3]	000_B	WL = 4
RL	MR2 OP[2:0]	000_B	RL = 6, nRTP = 8
nWR	MR1 OP[6:4]	000_B	nWR = 6
DBI-WR/RD	MR3 OP[7:6]	00_B	Write & Read DBI are disabled
CA ODT	MR11 OP[6:4]	000_B	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000_B	DQ ODT is disabled
V_{REFCA} Setting	MR12 OP[6]	1_B	V_{REFCA} Range[1] enabled
V_{REFCA} Value	MR12 OP[5:0]	011101_B	Range1: 50.4% of V_{DD2}
V_{REFDQ} Setting	MR14 OP[6]	1_B	V_{REFDQ} Range[1] enabled
V_{REFDQ} Value	MR14 OP[5:0]	011101_B	Range1: 50.4% of V_{DDQ}

Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR4 device. Unless specified otherwise, these steps are mandatory. Note that the power-up sequence of all channels must proceed simultaneously.

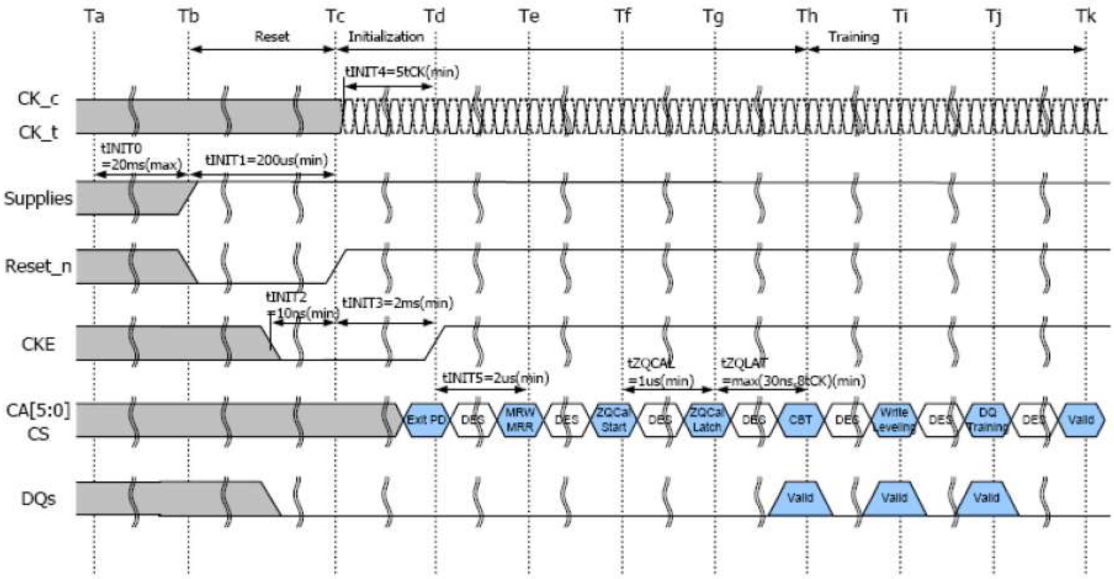
1. While applying power (after Ta), RESET_n is recommended to be LOW (≤0.2 x V_{DD2}) and all other inputs must be between $V_{IL(min)}$ and $V_{IH(max)}$. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 8. V_{DD1} must ramp at the same time or earlier than V_{DD2}. V_{DD2} must ramp at the same time or earlier than V_{DDQ}.

After	Applicable Condition
Ta is reached	V_{DD1} must be greater than V_{DD2}
	V_{DD2} must be greater than V_{DDQ} – 200mV

Note:
1. Ta is the point when any power supply first reaches 300mV.
2. Voltage ramp conditions in above table apply between Ta and power-off (controlled or uncontrolled).
3. Tb is the point at which all supply and reference voltages are within their defined ranges.
4. Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.
5. The voltage difference between any V_{SS} and V_{SSQ} pins must not excess 100mV.

2. Following the completion of the voltage ramp (Tb), RESET_n must be maintained LOW. DQ, DMI, DQS_t and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latch-up. CKE, CK_t, CK_c, CS_n and CA input levels must be between V_{SS} and V_{DD2} during voltage ramp to avoid latch-up.

3. Beginning at Tb, RESET_n must remain LOW for at least tINIT1(Tc), after which RESET_n can be de-asserted to HIGH(Tc). At least 10ns before CKE de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care".



Note:

1. Training is optional and may be done at the system architects discretion. The training sequence after ZQ_CAL Latch (The Sequence7~9) in the above figure, is simplified recommendation and actual training sequence may vary depending on systems.

4. After RESET_n is de-asserted (Tc), wait at least tINIT3 before activating CKE. Clock (CK_t,CK_c) is required to be start- ed and stabilized for tINIT4 before CKE goes active(Td). CS is required to be maintained LOW when controller activates CKE.
5. After setting CKE high, wait minimum of tINIT5 to issue any MRR or MRW commands (Te). For both MRR and MRW commands, the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured.
6. After completing all MRW commands to set the Pull-up, Pull-down and Rx termination values, the DRAM controller can issue ZQCAL Start command to the memory (Tf). This command is used to calibrate VOH level and output impedance over process, voltage and temperature. In systems where more than one LPDDR4 DRAM devices share one external ZQ resistor, the controller must not overlap the ZQ calibration sequence of each LPDDR4 device. ZQ calibration sequence is completed after tZQCAL (Tg) and the ZQCAL Latch command must be issued to update the DQ drivers and DQ+CA ODT to the calibrated values.
7. After tZQLAT is satisfied (Th) the command bus (internal V_{REFCA}, CS, and CA) should be trained for high-speed operation by issuing an MRW command (Command Bus Training Mode). This command is used to calibrate the device's internal V_{REF} and align CS/CA with CK for high-speed operation. The LPDDR4 device will power-up with receivers configured for low-speed operations, and V_{REFCA} set to a default factory setting. Normal device operation at clock speeds higher than tCKb may not be possible until command bus training has been completed. The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See command bus training in the MRW section for information on how to enter/ exit the training mode.
8. After command bus training, DRAM controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is high(Ti). See write leveling section for detailed description of write leveling entry and exit sequence. In write leveling mode, the DRAM controller adjusts write DQS_t/_c timing to the point where the LPDDR4 device recognizes the start of write DQ data burst with desired write latency.
9. After write leveling, the DQ Bus (internal V_{REFDQ}, DQS, and DQ) should be trained for high-speed operation using the MPC training commands and by issuing MRW commands to adjust V_{REFDQ} (Tj). The LPDDR4 device will power-up with receivers configured for low-speed operations and V_{REFDQ} set to a default factory setting. Normal device operation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The MPC Read Calibration command is used together with MPC FIFO Write/Read commands to train DQ bus without disturbing the memory array contents. See DQ Bus Training section for detailed DQ Bus Training sequence.

10. At Tk the LPDDR4 device is ready for normal operation and is ready to accept any valid command. Any more registers that have not previously been set up for normal operation should be written at this time.

Parameter	Value		Unit	Comment
	Min	Max		
tINIT0		20	ms	Maximum Voltage Ramp Time
tINIT1	200		us	Minimum RESET_N Low time after completion of voltage ramp
tINIT2	10		ns	Minimum CKE Low time before RESET_n goes High
tINIT3	2		ms	Minimum CKE Low time after RESET_n goes High
tINIT4	5		tCK	Minimum stable clock before first CKE High
tINIT5	2		us	Minimum idle time before first MRW/MRR command
tZQCAL	1		us	ZQ Calibration time
tZQLAT	Max(30ns, 80tCK)		ns	ZQCAL latch quite time
tCKb	Note 1,2	Note 1,2	ns	Clock cycle time during boot

Note:
1. Min tCKb guaranteed by DRAM test is 18ns.
2. The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent.

Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET_n below 0.2 x V_{DD2} anytime when reset is needed. RESET_n needs to be maintained for minimum tPW_RESET. CKE must be pulled Low at least 10ns before de-asserting RESET_n.
2. Repeat steps 4 to 10 in “Voltage Ramp and Device Initialization” section.

Parameter	Value		Unit	Comment
	Min	Max		
tIPW_RESET	100	-	ns	Minimum RESET_n low time for Reset Initialization with stable power

Power-off Sequence

The following procedure is required to power off the device.

While powering off, CKE must be held LOW (≤0.2 X V_{DD2}) and all other inputs must be between $V_{IL(min)}$ and $V_{IH(max)}$. The device’s output remains at High-Z while CKE is held LOW. DQ, DMI, DQS_t and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latch-up. RESET_n, CK_t, CK_c, CS and CA input levels must be between V_{SS} and V_{DD2} during voltage ramp to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.
Tz is the point where all power supplies are below 300mV. After TZ, the device is powered off.

Between	Applicable Conditions
Tx and Tx	V_{DD1} must be greater than V_{DD2}
	V_{DD2} must be greater than V_{DDQ} – 200mV

Note:
1. The voltage difference between any of V_{SS}, V_{SSQ} pins must not exceed 100mV

Uncontrolled Power-off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power supply current capacity must be at zero, except any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period the relative voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than 0.5 V/µs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Symbol	Value		Unit	Comment
	Min	Max		
tPOFF	-	2	s	Maximum Power-off ramp item

Mode Register Definition

Mode Register Assignment and Definition in LPDDR4x SDRAM

Below table shows the mode registers for LPDDR4 SDRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

<table>
<tr><th>MR#</th><th>Access</th><th>OP7</th><th>OP6</th><th>OP5</th><th>OP4</th><th>OP3</th><th>OP2</th><th>OP1</th><th>OP0</th></tr>
<tr><td>0</td><td>R</td><td>CATR</td><td colspan="2">RFU</td><td colspan="2">RZQI</td><td colspan="2">RFU</td><td>Refresh mode</td></tr>
<tr><td>1</td><td>W</td><td>RPST</td><td colspan="3">nWR</td><td>RD-PRE</td><td>WR-PRE</td><td colspan="2">BL</td></tr>
<tr><td>2</td><td>W</td><td>WR Lev</td><td>WLS</td><td colspan="3">WL</td><td colspan="3">RL</td></tr>
<tr><td>3</td><td>W</td><td>DBI-WR</td><td>DBI-RD</td><td colspan="3">PDDS</td><td>PPRP</td><td>WR PST</td><td>PU-CAL</td></tr>
<tr><td>4</td><td>R/W</td><td>TUF</td><td colspan="2">Thermal Offset</td><td>PPRE</td><td>SR Abort</td><td colspan="3">Refresh Rate</td></tr>
<tr><td>5</td><td>R</td><td colspan="8">LPDDR4x Manufacturer ID</td></tr>
<tr><td>6</td><td>R</td><td colspan="8">Revision ID-1</td></tr>
<tr><td>7</td><td>R</td><td colspan="7">Revision ID-2</td><td>Single-ended mode</td></tr>
<tr><td>8</td><td>R</td><td colspan="2">I/O Width</td><td colspan="4">Density</td><td colspan="2">Type</td></tr>
<tr><td>9</td><td>W</td><td colspan="8">Vendor Specific Test Register</td></tr>
<tr><td>10</td><td>W</td><td colspan="7">RFU</td><td>ZQ-Reset</td></tr>
<tr><td>11</td><td>W</td><td>RFU</td><td colspan="3">CA ODT</td><td>RFU</td><td colspan="3">DQ ODT</td></tr>
<tr><td>12</td><td>R/W</td><td>RFU</td><td>VR-CA</td><td colspan="6">V_{REFCA}</td></tr>
<tr><td>13</td><td>W</td><td>FSP-OP</td><td>FSP-WR</td><td>DMD</td><td>RRO</td><td>VRCG</td><td>VRO</td><td>RPT</td><td>CBT</td></tr>
<tr><td>14</td><td>R/W</td><td>RFU</td><td>VR-DQ</td><td colspan="6">V_{REFDQ}</td></tr>
<tr><td>15</td><td>W</td><td colspan="8">Lower-Byte Invert Register for DQ Calibration</td></tr>
<tr><td>16</td><td>W</td><td colspan="8">PASR Bank Mask</td></tr>
<tr><td>17</td><td>W</td><td colspan="8">PASR Segment Mask</td></tr>
<tr><td>18</td><td>R</td><td colspan="8">DQS Oscillator Count – LSB</td></tr>
<tr><td>19</td><td>R</td><td colspan="8">DQS Oscillator Count – MSB</td></tr>
<tr><td>20</td><td>W</td><td colspan="8">Upper-Byte Invert Register for DQ Calibration</td></tr>
<tr><td>21</td><td>N/A</td><td colspan="8">RFU</td></tr>
<tr><td>22</td><td>W</td><td colspan="2">RFU</td><td>ODT-CA</td><td>ODT-CS</td><td>ODT-CK</td><td colspan="3">SoC ODT</td></tr>
<tr><td>23</td><td>W</td><td colspan="8">DQS Interval Timer Run Time Setting</td></tr>
<tr><td>24</td><td>R/W</td><td>TRR mode</td><td colspan="3">TRR mode BAn</td><td>Unlimited MAC</td><td colspan="3">MAC Value</td></tr>
<tr><td>25</td><td>R</td><td>Bank 7</td><td>Bank 6</td><td>Bank 5</td><td>Bank 4</td><td>Bank 3</td><td>Bank 2</td><td>Bank 1</td><td>Bank 0</td></tr>
<tr><td>26:29</td><td>N/A</td><td colspan="8">RFU</td></tr>
<tr><td>30</td><td>N/A</td><td colspan="8">Reserved for Testing – SDRAM will ignore</td></tr>
<tr><td>31</td><td>N/A</td><td colspan="8">RFU</td></tr>
<tr><td>32</td><td>W</td><td colspan="8">DQ Calibration Pattern “A” (Default = $5A_H$)</td></tr>
<tr><td>33:38</td><td>N/A</td><td colspan="8">Do Not Use</td></tr>
<tr><td>39</td><td>N/A</td><td colspan="8">Reserved for Testing – SDRAM will ignore</td></tr>
<tr><td>40</td><td>W</td><td colspan="8">DQ Calibration Pattern “B” (Default = $3C_H$)</td></tr>
<tr><td>41:47</td><td>N/A</td><td colspan="8">Do Not Use</td></tr>
<tr><td>48:50</td><td>N/A</td><td colspan="8">RFU</td></tr>
<tr><td>51</td><td>W</td><td colspan="4">RFU</td><td>Single-ended Clock</td><td>Single-ended WDQS</td><td>Single-ended RDQS</td><td>RFU</td></tr>
<tr><td>52:63</td><td>N/A</td><td colspan="8">RFU</td></tr>
</table>

Note:
1. RFU bits shall be set to ‘0’ during write.
2. RFU bits shall be read as ‘0’ during read.
3. All mode registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.
4. All mode registers that are specified as RFU shall not be written.
5. Write to read-only registers shall have no impact on the functionality of the device.

MR0 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
CATR	RFU		RZQI		RFU		Refresh mode

Function	Register Type	Operand	Data	Note
Refresh mode	Read-only	OP[0]	**0$_B$**: Both legacy & modified refresh mode supported **1$_B$**: Only modified refresh mode supported	
RZQI (Built-in Self-Test for RZQ)		OP[4:3]	**00$_B$**: RZQ self-test not supported **01$_B$**: ZQ-pin may connect to V_{SSQ} or float **10$_B$**: ZQ-pin may short to V_{DDQ} **11$_B$**: ZQ-pin self-test completed, no error condition detected (ZQ-pin may not connect to V_{SSQ} or float, nor short to V_{DDQ})	1,2,3,4
CATR (CA Terminating Rank)		OP[7]	**0$_B$**: CA for this rank is not terminated **1$_B$**: Vendor specific	5

Note:

1. RZQI MR value, if supported, will be valid after the following sequence:
   a) Completion of MPC ZQCAL Start command to either channel.
   b) Completion of MPC ZQCAL Latch command to either channel then tZQLAT is satisfied. RZQI value will be lost after Reset.
2. If the ZQ-pin is connected to V_{SSQ} to set default calibration, OP[4:3] shall be set to 01B. If the ZQ-pin is not connected to V_{SSQ}, either OP[4:3] = 01B or OP[4:3] =10B might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3. In the case of possible assembly error, the LPDDR4x device will default to factory trim settings for RON and will ignore ZQ calibration commands. In either case, the device may not function as intended.
4. In ZQ self-test returns OP[4:3] = 11B, the device has detected a resistor connected to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e 240ohm ± 1%).
5. CATR functionality is Vendor specific. CATR can either indicate the connection status of the ODTCA pad for the die or whether CA for the rank is terminated. Consult the vendor device datasheet for details.

MR1 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RPST	nWR (for AP)			RD-PRE	WR-PRE	BL	

Function	Register Type	Operand	Data	Note
BL (Burst Length)	Write-only	OP[1:0]	**00_B**: BL=16 Sequential (Default) **01_B**: BL=32 Sequential **10_B**: BL=16 or 32 Sequential (on-the-fly) **All others**: Reserved	1
WR-PRE (WR Pre-amble Length)		OP[2]	**0_B**: Reserved **1_B**: WR Pre-amble = 2 x tCK	5,6
RD-PRE (RD Pre-amble Type)		OP[3]	**0_B**: RD Pre-amble = Static (Default) **1_B**: RD Pre-amble = Toggle	3,5,6
nWR (Write-Recovery for Auto-Precharge commands)		OP[6:4]	**000_B**: nWR = 6 (Default) **001_B**: nWR = 10 **010_B**: nWR = 16 **011_B**: nWR = 20 **100_B**: nWR = 24 **101_B**: nWR = 30 **110_B**: nWR = 34 **111_B**: nWR = 40	2,5,6
RPST (RD Post-amble Length)		OP[7]	**0_B**: RD Post-amble = 0.5 x tCK (Default) **1_B**: RD Post-amble = 1.5 x tCK	4,5,6

Note:

1. Burst length on-the-fly can be set to either BL=16 or BL=32 by setting the “BL” bit in the command operands. See the Command Truth Table.
2. The programmed value of nWR is the number of clock cycles the LPDDR4x device uses to determine the starting point of an internal Precharge operation after a Write burst with AP (auto-precharge) enabled. See, "Frequency Ranges for RL, WL, and nWR Settings" later in this section.
3. For Read operations this bit must be set to select between a “toggling” pre-amble and a “non-toggling” pre-amble. See the Read Pre-amble and Post-amble section in Operation timing for a drawing of each type of pre-amble.
4. OP[7] provides an optional READ post-amble with an additional rising and falling edge of DQS_t. The optional post-amble cycle is provided for the benefit of certain memory controllers.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.
7. Supporting the two physical registers for Burst Length: MR1 OP[1:0] as optional feature. Applications requiring support of both vendor options shall assure that both FSP-OP[0] and FSP-OP[1] are set to the same code. Refer to vendor datasheets for detail.

Read and Write Latencies

Read Latency		Write Latency		nWR	nRTP	Lower Clock Frequency Limit (Greater than)	Upper Clock Frequency Limit (Same or Less than)	Unit	Note
No DBI	w/ DBI	Set “A”	Set “B”						
6	6	4	4	6	8	10	266	MHz	1,2,3, 4,5,6
10	12	6	8	10	8	266	533		
14	16	8	12	16	8	533	800		
20	22	10	18	20	8	800	1066		
24	28	12	22	24	10	1066	1333		
28	32	14	26	30	12	1333	1600		
32	36	16	30	34	14	1600	1866		
36	40	18	34	40	16	1866	2133		

Note:

1. The LPDDR4x device should not be operated at a frequency above the Upper Frequency Limit, or below the Lower Frequency Limit, shown for each RL, WL, nRTP, or nWR value.
2. DBI for Read operations is enabled in MR3 OP[6]. When MR3 OP[6]=0B, then the “No DBI” column should be used for Read Latency. When MR3 OP[6]=1B, then the “w/DBI” column should be used for Read Latency.
3. Write Latency Set “A” and Set “B” is determined by MR2 OP[6]. When MR2 OP[6]=0B, then Write Latency Set “A” should be used. When MR2 OP[6]=1B, then Write Latency Set “B” should be used.
4. The programmed value of nWR is the number of clock cycles the LPDDR4x device uses to determine the starting point of an internal Precharge operation after a Write burst with AP (auto precharge). It is determined by RU(tWR/tCK).
5. The programmed value of nRTP is the number of clock cycles the LPDDR4x device uses to determine the starting point of an internal Precharge operation after a Read burst with AP (auto precharge). It is determined by RU(tRTP/tCK).
6. nRTP shown in this table is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the nRTP value before starting a precharge.

Burst Sequence for READ

BL	BT	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																													
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	Seq	V	0_B	0_B	0_B	0_B	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
		V	0_B	1_B	0_B	0_B	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3																
		V	1_B	0_B	0_B	0_B	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7																
		V	1_B	1_B	0_B	0_B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B																
32	Seq	0_B	0_B	0_B	0_B	0_B	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
		0_B	0_B	1_B	0_B	0_B	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13
		0_B	1_B	0_B	0_B	0_B	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17
		0_B	1_B	1_B	0_B	0_B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B
		1_B	0_B	0_B	0_B	0_B	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		1_B	0_B	1_B	0_B	0_B	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		1_B	1_B	0_B	0_B	0_B	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1_B	1_B	1_B	0_B	0_B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B

Note:
1. C0-C1 are assumed to be "0" and are not transmitted on the command bus.
2. The starting burst address is on 64-bit (4n) boundaries

Burst Sequence for Write

BL	BT	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																													
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	Seq	V	0_B	0_B	0_B	0_B	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
32	Seq	0_B	0_B	0_B	0_B	0_B	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

Note:
1. C0-C1 are assumed to be "0" and are not transmitted on the command bus.
2. The starting address is on 256-bit (16n) boundaries for Burst Length 16.
3. The starting address is on 512-bit (32n) boundaries for Burst Length 32.
4. C2-C3 shall be set to "0" for all Write Operation.

MR2 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WR Lev	WLS	WL			RL		

Function	Register Type	Operand	Data	Note
RL (Read Latency)	Write-only	OP[2:0]	**RL & nRTP for DBI-RD Disabled (MR3 OP[6] = 0B)** **000B**: RL=6, nRTP=8 (Default) **001B**: RL=10, nRTP=8 **010B**: RL=14, nRTP=8 **011B**: RL=20, nRTP=8 **100B**: RL=24, nRTP=10 **101B**: RL=28, nRTP=12 **110B**: RL=32, nRTP=14 **111B**: RL=36, nRTP=16 **RL & nRTP for DBI-RD Enabled (MR3 OP[6] = 1B)** **000B**: RL=6, nRTP=8 **001B**: RL=12, nRTP=8 **010B**: RL=16, nRTP=8 **011B**: RL=22, nRTP=8 **100B**: RL=28, nRTP=10 **101B**: RL=32, nRTP=12 **110B**: RL=36, nRTP=14 **111B**: RL=40, nRTP=16	1,3,4
WL (Write Latency)		OP[5:3]	**WL Set "A" (MR2 OP[6] = 0B)** **000B**: WL=4 (Default) **001B**: WL=6 **010B**: WL=8 **011B**: WL=10 **100B**: WL=12 **101B**: WL=14 **110B**: WL=16 **111B**: WL=18 **WL Set "B" (MR2 OP[6] = 1B)** **000B**: WL=4 **001B**: WL=8 **010B**: WL=12 **011B**: WL=18 **100B**: WL=22 **101B**: WL=26 **110B**: WL=30 **111B**: WL=34	1,3,4
WLS (Write Latency Set)		OP[6]	**0B**: WL Set "A" (Default) **1B**: WL Set "B"	1,3,4
WR Leveling		OP[7]	**0B**: Disabled (Default) **1B**: Enabled	2

Note:

1. See Latency Code Frequency Table for allowable frequency ranges for RL/WL/nWR/nRTP.
2. After a MRW to set the Write Leveling Enable bit (OP[7]=1B), the LPDDR4x device remains in the MRW state until another MRW command clears the bit (OP[7]=0B). No other commands are allowed until the Write Leveling Enable bit is cleared.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
4. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

MR3 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DBI-WR	DBI-RD	PDDS			PPRP	WR PST	PU-CAL

Function	Register Type	Operand	Data	Note
PU-CAL (Pull-Up Calibration Point)	Write-only	OP[0]	**0**$_B$: V_{DDQ} x 0.6 **1**$_B$: V_{DDQ} x 0.5 (Default)	1,4
WR PST (WR Post-amble Length)		OP[1]	**0**$_B$: WR Post-amble = 0.5 x tCK (Default) **1**$_B$: WR Post-amble = 1.5 x tCK (Vendor Specific Function)	2,3,5
Post Package Repair Protection		OP[2]	**0**$_B$: PPR Protection disabled (Default) **1**$_B$: PPR Protection enabled	6
PDDS (Pull-Down Drive Strength)		OP[5:3]	**000**$_B$: RFU **001**$_B$: RZQ/1 **010**$_B$: RZQ/2 **011**$_B$: RZQ/3 **100**$_B$: RZQ/4 **101**$_B$: RZQ/5 **110**$_B$: RZQ/6 (Default) **111**$_B$: Reserved	1,2,3
DBI-RD (DBI-Read Enable)		OP[6]	**0**$_B$: Disabled (Default) **1**$_B$: Enabled	2,3
DBI-WR (DBI-Write Enable)		OP[7]	**0**$_B$: Disabled (Default) **1**$_B$: Enabled	2,3

Note:
1. All values are “typical”. The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.
4. For dual channel devices, PU-CAL setting is required as the same value for both Ch A and Ch B before issuing ZQ Cal start command.
5. Refer to the supplier data sheet for vender specific function. 1.5 x tCK apply > 1.6GHz clock.
6. If MR3 OP[2] is set to 1b then PPR protection mode is enabled. The PPR Protection bit is a sticky bit and can only be set to 0b by a power on reset. MR4 OP[4] controls entry to PPR Mode. If PPR protection is enabled then DRAM will not allow writing of 1 to MR4 OP[4].

MR4 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	Thermal Offset		PPRE	SR Abort	Refresh Rate		

Function	Register Type	Operand	Data	Note
Refresh Rate	Read-only	OP[2:0]	**000$_B$**: SDRAM Low Temperature Operating Limit Exceeded **001$_B$**: 4x Refresh **010$_B$**: 2x Refresh **011$_B$**: 1x Refresh (Default) **100$_B$**: 0.5x Refresh **101$_B$**: 0.25x Refresh, no de-rating **110$_B$**: 0.25x Refresh, with de-rating **111$_B$**: SDRAM High Temperature Operating Limit Exceeded	1,2,3,4, 7,8,9
SR Abort (Self-Refresh Abort)	Write-only	OP[3]	**0$_B$**: Disabled (Default) **1$_B$**: Enabled	9,11
PPRE (Post-Package Repair Entry/Exit)	Write-only	OP[4]	**0$_B$**: Exit PPR mode (Default) **1$_B$**: Enter PPR mode	5,9
Thermal Offset (Vendor Specific Function)	Write-only	OP[6:5]	**00$_B$**: No offset, 0 ~ 5℃ gradient (Default) **01$_B$**: 5℃ offset, 5 ~ 10℃ gradient **10$_B$**: 10℃ offset, 10 ~ 15℃ gradient **11$_B$**: Reserved	10
TUF (Temperature Update Flag)	Read-only	OP[7]	**0$_B$**: No change in OP[2:0] since last MR4 read (Default) **1$_B$**: Change in OP[2:0] since last MR4 read	6,7,8

Note:

1. The refresh rate for each MR4 OP[2:0] setting applies to tREFI, tREFIpb and tREFW. OP[2:0]=011B corresponds to a device temperature of 85°C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures, or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If OP[2]=1$_B$, the device temperature is greater than 85°C.
2. At higher temperatures (>95°C), AC timing derating may be required. If derating is required the LPDDR4x will set OP[2:0]=110$_B$. See derating timing requirements in the AC Timing section.
3. DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
4. The device may not operate properly when OP[2:0]=000$_B$ or 111$_B$.
5. Post-package repair can be entered or exited by writing to OP[4].
6. When OP[7]=1$_B$, the refresh rate reported in OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to '0'.
7. OP[7]=0$_B$ at power-up. OP[2:0] bits are valid after initialization sequence (Te).
8. See the section on "Temperature Sensor" for information on the recommended frequency of reading MR4.
9. OP[6:3] bits that can be written in this register. All other bits will be ignored by the DRAM during a MRW to this register.
10. Refer to the supplier data sheet for vender specific function.

MR5 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR4x Manufacturer ID							

Function	Register Type	Operand	Data	Note
LPDDR4x Manufacturer ID	Read-only	OP[7:0]	**0000 0001$_B$**: SEC	

MR6 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID-1							

Function	Register Type	Operand	Data	Note
LPDDR4x Revision ID-1	Read-only	OP[7:0]	**0000 0110$_B$**: G-version	1

Note:

1. MR6 is vendor specific.

MR7 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID-2							Single-ended mode

Function	Register Type	Operand	Data	Note
LPDDR4x Revision ID-2	Read-only	OP[7:1]	**0000 000$_B$**	1
Single-ended mode		OP[0]	**0$_B$**: Not support for Single-ended mode **1$_B$**: Support for Single-ended mode	2

Note:
1. MR7 is vendor specific.
2. Support for Single-ended mode is optional. If supported, Single-ended Write DQS, Read DQS and CK can be enabled in MR51.

MR8 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O Width		Density				Type	

Function	Register Type	Operand	Data	Note
Type	Read-only	OP[1:0]	**00$_B$**: LPDDR4 S16 SDRAM (16n pre-fetch) Standard V_{DDQ} (1.1v) only **10$_B$**: LPDDR4x S16 SDRAM (16n pre-fetch) Low V_{DDQ} (0.6v) only **Others:** Reserved	
Density		OP[5:2]	**0000$_B$**: 4Gb Dual Channel die / 2Gb Single Channel die **0001$_B$**: 6Gb Dual Channel die / 3Gb Single Channel die **0010$_B$**: 8Gb Dual Channel die / 4Gb Single Channel die **0011$_B$**: 12Gb Dual Channel die / 6Gb Single Channel die **0100$_B$**: 16Gb Dual Channel die / 8Gb Single Channel die **0101$_B$**: 24Gb Dual Channel die / 12Gb Single Channel die **0110$_B$**: 32Gb Dual Channel die / 16Gb Single Channel die **Others**: Reserved	
I/O Width		OP[7:6]	**00$_B$**: x16 (per channel) **Others**: Reserved	

MR9 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-Specific Test Register							

Note:
1. Only 00$_H$ should be written to this Register

MR10 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU							ZQ-Reset

Function	Register Type	Operand	Data	Note
ZQ-Reset	Write-only	OP[0]	**0$_B$**: Normal Operation (Default) **1$_B$**: ZQ Reset	1,2

Note:
1. See the AC Timing tables for calibration latency and timing
2. If the ZQ-pin is connected to V_{DDQ} through RZQ, either the ZQ calibration function or default calibration (via ZQ-Reset) is supported. If the ZQ-pin is connected to V_{SS}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

MR11 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	CA ODT			RFU	DQ ODT		

Function	Register Type	Operand	Data	Note
DQ ODT (DQ Bus Receiver On-Die-Termination)	Write-only	OP[2:0]	**000B**: Disable (Default) **001B**: RZQ/1 **010B**: RZQ/2 **011B**: RZQ/3 **100B**: RZQ/4 **101B**: RZQ/5 **110B**: RZQ/6 **111B**: RFU	1,2,3
CA ODT (CA Bus Receiver On-Die-Termination		OP[4:6]	**000B**: Disable (Default) **001B**: RZQ/1 **010B**: RZQ/2 **011B**: RZQ/3 **100B**: RZQ/4 **101B**: RZQ/5 **110B**: RZQ/6 **111B**: RFU	1,2,3

Note:

1. All values are “typical”. The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

MR12 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	VR-CA	V_{REFCA}					

Function	Register Type	Operand	Data	Note
V_{REFCA} (V_{REFCA} Setting)	Read/Write	OP[5:0]	**00 0000$_B$**: --- Thru --- **11 0010$_B$**: See table below **Others**: Reserved	1,2,3,4, 5,6
V_{REFCA} (V_{REFCA} Range)		OP[6]	**0$_B$**: V_{REFCA} Range[0] enabled **1$_B$**: V_{REFCA} Range[1] enabled (Default)	1,2,3,4, 5,6

Note:

1. This register controls the V_{REFCA} levels.
2. A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.
3. A write to OP[5:0] sets the internal V_{REFCA} level for FSP[0] when MR13 OP[6]=0B, or sets FSP[1] when MR13 OP[6]=1B. The time required for V_{REFCA} to reach the set level depends on the step size from the current level to the new level. See the section on V_{REFCA} training for more information.
4. A write to OP[6] switches the LPDDR4x between two internal V_{REFCA} ranges. The range (Range[0] or Range[1]) must be selected when setting the V_{REFCA} register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

Function	Operand	Range[0] Values (% of V_{DDQ})		Range[1] Values (% of V_{DDQ})		Note
V_{REF} Setting for MR12	OP[5:0]	**000000$_B$**: 15.0%	**011010$_B$**: 30.0%	**000000$_B$**: 32.9%	**011010$_B$**: 48.5%	1,2,3
		000001$_B$: 15.6%	**011011$_B$**: 31.2%	**000001$_B$**: 33.5%	**011011$_B$**: 49.1%	
		000010$_B$: 16.2%	**011100$_B$**: 31.8%	**000010$_B$**: 34.1%	**011100$_B$**: 49.7%	
		000011$_B$: 16.8%	**011101$_B$**: 32.4%	**000011$_B$**: 34.7%	**011101$_B$**: 50.3% (Default)	
		000100$_B$: 17.4%	**011110$_B$**: 33.0%	**000100$_B$**: 35.3%	**011110$_B$**: 50.9%	
		000101$_B$: 18.0%	**011111$_B$**: 33.6%	**000101$_B$**: 35.9%	**011111$_B$**: 51.5%	
		000110$_B$: 18.6%	**100000$_B$**: 34.2%	**000110$_B$**: 36.5%	**100000$_B$**: 52.1%	
		000111$_B$: 19.2%	**100001$_B$**: 34.8%	**000111$_B$**: 37.1%	**100001$_B$**: 52.7%	
		001000$_B$: 19.8%	**100010$_B$**: 35.4%	**001000$_B$**: 37.7%	**100010$_B$**: 53.3%	
		001001$_B$: 20.4%	**100011$_B$**: 36.0%	**001001$_B$**: 38.3%	**100011$_B$**: 53.9%	
		001010$_B$: 21.0%	**100100$_B$**: 36.6%	**001010$_B$**: 38.9%	**100100$_B$**: 54.5%	
		001011$_B$: 21.6%	**100101$_B$**: 37.2%	**001011$_B$**: 39.5%	**100101$_B$**: 55.1%	
		001100$_B$: 22.2%	**100110$_B$**: 37.8%	**001100$_B$**: 40.1%	**100110$_B$**: 55.7%	
		001101$_B$: 22.8%	**100111$_B$**: 38.4%	**001101$_B$**: 40.7%	**100111$_B$**: 56.3%	
		001110$_B$: 23.4%	**101000$_B$**: 39.0%	**001110$_B$**: 41.3%	**101000$_B$**: 56.9%	
		001111$_B$: 24.0%	**101001$_B$**: 39.6%	**001111$_B$**: 41.9%	**101001$_B$**: 57.5%	
		010000$_B$: 24.6%	**101010$_B$**: 40.2%	**010000$_B$**: 42.5%	**101010$_B$**: 58.1%	
		010001$_B$: 25.2%	**101011$_B$**: 40.8%	**010001$_B$**: 43.1%	**101011$_B$**: 58.7%	
		010010$_B$: 25.8%	**101100$_B$**: 41.4%	**010010$_B$**: 43.7%	**101100$_B$**: 59.3%	
		010011$_B$: 26.4%	**101101$_B$**: 42.0%	**010011$_B$**: 44.3%	**101101$_B$**: 59.9%	
		010100$_B$: 27.0%	**101110$_B$**: 42.6%	**010100$_B$**: 44.9%	**101110$_B$**: 60.5%	
		010101$_B$: 27.6%	**101111$_B$**: 43.2%	**010101$_B$**: 45.5%	**101111$_B$**: 61.1%	
		010110$_B$: 28.2%	**110000$_B$**: 43.8%	**010110$_B$**: 46.1%	**110000$_B$**: 61.7%	
		010111$_B$: 28.8%	**110001$_B$**: 44.4%	**010111$_B$**: 46.7%	**110001$_B$**: 62.3%	
		011000$_B$: 29.4%	**110010$_B$**: 45.0%	**011000$_B$**: 47.3%	**110010$_B$**: 62.9%	
		011001$_B$: 30.0%	**Others**: Reserved	**011001$_B$**: 47.9%	**Others**: Reserved	

Note:

1. These values may be used for MR12 OP[5:0] to set the V_{REFCA} levels in the LPDDR4x.
2. The range may be selected in the MR12 register by setting OP[6] appropriately.
3. The MR12 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and unterminated operation, or between different high-frequency setting which may use different terminations values.

MR13 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT

Function	Register Type	Operand	Data	Note
CBT (Command Bus Training)	Write-only	OP[0]	**0**$_B$: Normal Operation (Default) **1**$_B$: Command Bus Training mode Enabled	1
RPT (Read Preamble Training)		OP[1]	**0**$_B$: Disable (Default) **1**$_B$: Enable	
VRO (V_{REF} Output)		OP[2]	**0**$_B$: Normal Operation (Default) **1**$_B$: Output the V_{REFCA} and V_{REFDQ} values on DQ bits	2
VRCG (V_{REF} Current Generator)		OP[3]	**0**$_B$: Normal Operation (Default) **1**$_B$: V_{REF} Fast Response (High Current) mode	3
RRO (Refresh Rate Option)		OP[4]	**0**$_B$: Disable codes 001 and 010 in MR4 OP[2:0] **1**$_B$: Enable all codes in MR4 OP[2:0]	4,5
DMD (Data Mask Disable)		OP[5]	**0**$_B$: Data Mask Operation Enabled (Default) **1**$_B$: Data Mask Operation Disabled	6
FSP-WR (Frequency Set Point Write/Read)		OP[6]	**0**$_B$: Frequency-Set-Point[0] (Default) **1**$_B$: Frequency-Set-Point[1]	7
FSP-OP (Frequency Set Point Operation mode)		OP[7]	**0**$_B$: Frequency-Set-Point[0] (Default) **1**$_B$: Frequency-Set-Point[1]	8

Note:

1. A write to set OP[0]=1$_B$ causes the LPDDR4x to enter the Command Bus training mode. When OP[0]=1$_B$ and CKE goes Low, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0]=0$_B$) and return to normal operation. See the Command Bus Training section for more information.
2. When set, the LPDDR4x will output the V_{REFCA} and V_{REFDQ} voltages on DQ pins. Only the "active" frequency-set-point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal V_{REF} levels. The DQ pins used for V_{REF} output are vendor specific.
3. When OP[3]=1$_B$, the V_{REF} circuit uses a high-current mode to improve V_{REF} settling time.
4. MR13 OP[4] RRO bit is valid only when MR0 OP[0]= 1$_B$. For LPDDR4x devices with MR0 OP[0] = 0$_B$, MR4 OP[2:0] bits are not dependent on MR13 OP4.
5. When OP[4] = 0$_B$, only 001$_B$ and 010$_B$ in MR4 OP[2:0] are disabled. LPDDR4x devices must report 011B instead of 001$_B$ or 010$_B$ in this case. Controller should follow the refresh mode reported by MR4 OP[2:0], regardless of RRO setting. TCSR function does not depend on RRO setting.
6. When enabled (OP[5]=0$_B$) data masking is enabled for the device. When disabled (OP[5]=1$_B$), masked write command is illegal. See LPDDR4x Data Mask (DM) and Data Bus Inversion (DBIdc) Function in operation timing datasheet.
7. FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions such as V_{REFCA} Setting, V_{REFCA} Range, V_{REFDQ} Setting, V_{REFDQ} Range. For more information, refer to Frequency Set Point section in operations and timing spec.
8. FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following functions such as V_{REFCA} Setting, V_{REFCA} Range, V_{REFDQ} Setting, V_{REFDQ} Range. For more information, refer to Frequency Set Point section in operations and timing spec.

MR14 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	VR-DQ	V_{REFDQ}					

Function	Register Type	Operand	Data	Note
V_{REFDQ} (V_{REFDQ} Setting)	Read/Write	OP[5:0]	**00 0000**$_B$: --- Thru --- **11 0010**$_B$: See table below **Others**: Reserved	1,2,3,4, 5,6
V_{REFDQ} (V_{REFDQ} Range)		OP[6]	**0**$_B$: V_{REFDQ} Range[0] enabled **1**$_B$: V_{REFDQ} Range[1] enabled (Default)	1,2,3,4, 5,6

Note:

1. This register controls the V_{REFDQ} levels for Frequency-Set-Point[1:0]. Values from either VR(DQ)[0] or VR(DQ)[1] may be selected by setting OP[6] appropriately.
2. A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.
3. A write to OP[5:0] sets the internal V_{REFDQ} level for FSP[0] when MR13 OP[6]=0B, or sets FSP[1] when MR13 OP[6]=1B. The time required for V_{REFDQ} to reach the set level depends on the step size from the current level to the new level. See the section on V_{REFDQ} training for more information.
4. A write to OP[6] switches the LPDDR4x between two internal V_{REFDQ} ranges. The range (Range[0] or Range[1]) must be selected when setting the V_{REFDQ} register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

Function	Operand	Range[0] Values (% of V_{DDQ})		Range[1] Values (% of V_{DDQ})		Note
V_{REF} Setting for MR14	OP[5:0]	**000000**$_B$: 15.0%	**011010**$_B$: 30.0%	**000000**$_B$: 32.9%	**011010**$_B$: 48.5%	1,2,3
		000001$_B$: 15.6%	**011011**$_B$: 31.2%	**000001**$_B$: 33.5%	**011011**$_B$: 49.1%	
		000010$_B$: 16.2%	**011100**$_B$: 31.8%	**000010**$_B$: 34.1%	**011100**$_B$: 49.7%	
		000011$_B$: 16.8%	**011101**$_B$: 32.4%	**000011**$_B$: 34.7%	**011101**$_B$: 50.3% (Default)	
		000100$_B$: 17.4%	**011110**$_B$: 33.0%	**000100**$_B$: 35.3%	**011110**$_B$: 50.9%	
		000101$_B$: 18.0%	**011111**$_B$: 33.6%	**000101**$_B$: 35.9%	**011111**$_B$: 51.5%	
		000110$_B$: 18.6%	**100000**$_B$: 34.2%	**000110**$_B$: 36.5%	**100000**$_B$: 52.1%	
		000111$_B$: 19.2%	**100001**$_B$: 34.8%	**000111**$_B$: 37.1%	**100001**$_B$: 52.7%	
		001000$_B$: 19.8%	**100010**$_B$: 35.4%	**001000**$_B$: 37.7%	**100010**$_B$: 53.3%	
		001001$_B$: 20.4%	**100011**$_B$: 36.0%	**001001**$_B$: 38.3%	**100011**$_B$: 53.9%	
		001010$_B$: 21.0%	**100100**$_B$: 36.6%	**001010**$_B$: 38.9%	**100100**$_B$: 54.5%	
		001011$_B$: 21.6%	**100101**$_B$: 37.2%	**001011**$_B$: 39.5%	**100101**$_B$: 55.1%	
		001100$_B$: 22.2%	**100110**$_B$: 37.8%	**001100**$_B$: 40.1%	**100110**$_B$: 55.7%	
		001101$_B$: 22.8%	**100111**$_B$: 38.4%	**001101**$_B$: 40.7%	**100111**$_B$: 56.3%	
		001110$_B$: 23.4%	**101000**$_B$: 39.0%	**001110**$_B$: 41.3%	**101000**$_B$: 56.9%	
		001111$_B$: 24.0%	**101001**$_B$: 39.6%	**001111**$_B$: 41.9%	**101001**$_B$: 57.5%	
		010000$_B$: 24.6%	**101010**$_B$: 40.2%	**010000**$_B$: 42.5%	**101010**$_B$: 58.1%	
		010001$_B$: 25.2%	**101011**$_B$: 40.8%	**010001**$_B$: 43.1%	**101011**$_B$: 58.7%	
		010010$_B$: 25.8%	**101100**$_B$: 41.4%	**010010**$_B$: 43.7%	**101100**$_B$: 59.3%	
		010011$_B$: 26.4%	**101101**$_B$: 42.0%	**010011**$_B$: 44.3%	**101101**$_B$: 59.9%	
		010100$_B$: 27.0%	**101110**$_B$: 42.6%	**010100**$_B$: 44.9%	**101110**$_B$: 60.5%	
		010101$_B$: 27.6%	**101111**$_B$: 43.2%	**010101**$_B$: 45.5%	**101111**$_B$: 61.1%	
		010110$_B$: 28.2%	**110000**$_B$: 43.8%	**010110**$_B$: 46.1%	**110000**$_B$: 61.7%	
		010111$_B$: 28.8%	**110001**$_B$: 44.4%	**010111**$_B$: 46.7%	**110001**$_B$: 62.3%	
		011000$_B$: 29.4%	**110010**$_B$: 45.0%	**011000**$_B$: 47.3%	**110010**$_B$: 62.9%	
		011001$_B$: 30.0%	**Others**: Reserved	**011001**$_B$: 47.9%	**Others**: Reserved	

Note:

1. These values may be used for MR14 OP[5:0] to set the V_{REFDQ} levels in the LPDDR4x.
2. The range may be selected in the MR14 register by setting OP[6] appropriately.
3. The MR14 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and unterminated operation, or between different high-frequency setting which may use different terminations values.

MR15 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Lower-Byte Invert Register for DQ Calibration							

Function	Register Type	Operand	Data	Note
Lower-Byte Invert Register for DQ Calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane: **0**$_B$: Do not invert **1**$_B$: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55$_H$	1,2,3

Note:
1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR15 OP[7:0]=00010101$_B$, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted.
2. DMI[0] is not inverted, and always transmits the "true" data contained in MR32/MR40.
3. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

Pin	DQ0	DQ1	DQ2	DQ3	DMI0	DQ4	DQ5	DQ6	DQ7
MR15	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

MR16 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR Bank Mask							

Function	Register Type	Operand	Data	Note
Bank[7:0] Mask	Write-only	OP[7:0]	**0**$_B$: Bank Refresh Enabled (Default): Unmasked **1**$_B$: Bank Refresh Disabled: Masked	1

OP	Bank Mask	8-Bank SDRAM
0	XXXX XXX1	Bank 0
1	XXXX XX1X	Bank 1
2	XXXX X1XX	Bank 2
3	XXXX 1XXX	Bank 3
4	XXX1 XXXX	Bank 4
5	XX1X XXXX	Bank 5
6	X1XX XXXX	Bank 6
7	1XXX XXXX	Bank 7

Note:
1. When a mask bit is asserted (OP[n]=1), refresh to that bank is disabled.
2. PASR bank-masking is on a per-channel basis. The two channels on the die may have different bank masking in dual channel devices.

MR17 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR Segment Mask							

Function	Register Type	Operand	Data	Note
PASR Segment Mask	Write-only	OP[7:0]	**0**$_B$: Segment Refresh Enabled (Default) **1**$_B$: Segment Refresh Disabled	

Segment	OP	Segment Mask	2Gb per Channel	3Gb per Channel	4Gb per Channel	6Gb per Channel	8Gb per Channel	12Gb per Channel	16Gb per Channel
			R13:11	R14:12	R14:12	R15:13	R15:13	R16:14	R16:14
0	0	XXXX XXX1	**000**$_B$						
1	1	XXXX XX1X	**001**$_B$						
2	2	XXXX X1XX	**010**$_B$						
3	3	XXXX 1XXX	**011**$_B$						
4	4	XXX1 XXXX	**100**$_B$						
5	5	XX1X XXXX	**101**$_B$						
6	6	X1XX XXXX	**110**$_B$	**Not Allowed**	**110**$_B$	**Not Allowed**	**110**$_B$	**Not Allowed**	**110**$_B$
7	7	1XXX XXXX	**111**$_B$		**111**$_B$		**111**$_B$		**111**$_B$

Note:
1. This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular segment.
2. PASR segment-masking is on a per-channel basis. The two channels on the die may have different segment masking in dual channel devices.
3. For 3Gb, 6Gb, and 12Gb per channel densities, OP[7:6] must always be LOW (=00_B).

MR18 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS Oscillator Count – LSB							

Function	Register Type	Operand	Data	Note
DQS Oscillator Count (WR Training DQS Oscillator)	Read-only	OP[7:0]	0-255 LSB DRAM DQS Oscillator Count	1,2,3

Note:
1. MR18 reports the LSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

MR19 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS Oscillator Count – MSB							

Function	Register Type	Operand	Data	Note
DQS Oscillator (WR Training DQS Oscillator)	Read-only	OP[7:0]	0-255 MSB DRAM DQS Oscillator Count	1,2,3

Note:
1. MR19 reports the MSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

MR20 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Upper-Byte Invert Register for DQ Calibration							

Function	Register Type	Operand	Data	Note
Upper-Byte Invert for DQ Calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane: **0**$_B$: Do not invert **1**$_B$: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55$_H$	1,2

Note:

1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR20 OP[7:0]=00010101$_B$, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be inverted.
2. DMI[1] is not inverted, and always transmits the "true" data contained in MR32/MR40.
3. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

Pin	DQ8	DQ9	DQ10	DQ11	DMI1	DQ12	DQ13	DQ14	DQ15
MR20	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

MR21 Register Information

Reserved for Future Use

MR22 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		ODT-CA	ODT-CS	ODT-CK	SoC ODT		

Function	Register Type	Operand	Data	Note
SoC ODT (Controller ODT value for V_{OH} Calibration)	Write-only	OP[2:0]	**000$_B$**: Disable (Default) **001$_B$**: RZQ/1 (Illegal if MR3 OP0 = 0$_B$) **010$_B$**: RZQ/2 **011$_B$**: RZQ/3 (Illegal if MR3 OP0 = 0$_B$) **100$_B$**: RZQ/4 **101$_B$**: RZQ/5 (Illegal if MR3 OP0 = 0$_B$) **110$_B$**: RZQ/6 (Illegal if MR3 OP0 = 0$_B$) **111$_B$**: RFU	1,2,3
ODT-CK		OP[3]	ODT bond PAD is ignored **0$_B$**: ODT-CK Enabled (Default) **1$_B$**: ODT-CK Disabled	2,3,4
ODT-CS		OP[4]	ODT bond PAD is ignored **0$_B$**: ODT-CS Enabled (Default) **1$_B$**: ODT-CS Disabled	2,3,4
ODTD-CA (CA ODT Termination Disable)		OP[5]	ODT bond PAD is ignored **0$_B$**: ODT-CA Obeys ODT_CA bond pad (Default) **1$_B$**: ODT-CS Disabled	2,3,4

Note:
1. All values are “typical”.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.
4. LPDDR4x device ignore ODT bond PAD

V_{OH} CAL (MR3 OP0)		SoC ODT Value (MR22 OP[2:0])							
		000$_B$	**001$_B$**	**010$_B$**	**011$_B$**	**100$_B$**	**101$_B$**	**110$_B$**	**111$_B$**
0$_B$ (V_{OH} = V_{DDQ} x 3/5)	SoC ODT	Disable	Illegal	RZQ/2 = 120ohm	Illegal	RZQ/4 = 60ohm	Illegal	Illegal	RFU
	DRAM Pull-Up	Default	N/A	RZQ/3 = 80ohm	N/A	RZQ/6 = 40ohm	N/A	N/A	RFU
1$_B$ (V_{OH} = V_{DDQ} / 2)	SoC ODT	Disable	RZQ/1 = 240ohm	RZQ/2 = 120ohm	RZQ/3 = 80ohm	RZQ/4 = 60ohm	RZQ/5 = 48ohm	RZQ/6 = 40ohm	RFU
	DRAM Pull-Up	Default	RZQ/1 = 240ohm	RZQ/2 = 120ohm	RZQ/3 = 80ohm	RZQ/4 = 60ohm	RZQ/5 = 48ohm	RZQ/6 = 40ohm	RFU

Note:
1. There is no corresponding RZQ/x value for 001$_B$, 011$_B$, 101$_B$, 110$_B$ when MR3 OP0 = 0$_B$ to support 3/5 V_{DDQ} V_{OH} value.

MR23 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS Interval Timer Run Time Setting							

Function	Register Type	Operand	Data	Note
DQS Interval Timer Run Time	Write-only	OP[7:0]	**0000 0000**$_B$: DQS Interval Timer stops via MPC Command (Default) **0000 0001**$_B$: DQS Timer stops automatically at 16th clocks after timer start **0000 0010**$_B$: DQS Timer stops automatically at 32th clocks after timer start **0000 0011**$_B$: DQS Timer stops automatically at 48th clocks after timer start **0000 0100**$_B$: DQS Timer stops automatically at 64th clocks after timer start ----------------------Thru---------------------- **0011 1111**$_B$: DQS Timer stops automatically at (63x16)th clocks after timer start **01XX XXXX**$_B$: DQS Timer stops automatically at 2048th clocks after timer start **10XX XXXX**$_B$: DQS Timer stops automatically at 4096th clocks after timer start **11XX XXXX**$_B$: DQS Timer stops automatically at 8192th clocks after timer start	1,2

Note:
1. MPC command with OP[6:0]=1001 101$_B$ (Stop DQS Interval Oscillator) stops DQS interval timer in case of MR23 OP[7:0] = 0000 0000$_B$.
2. MPC command with OP[6:0]=1001 101$_B$ (Stop DQS Interval Oscillator) is illegal with non-zero values in MR23 OP[7:0].

MR24 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TRR mode	TRR mode BAn			Unlimited MAC	MAC Value		

Function	Register Type	Operand	Data	Note
MAC Value	Read-only	OP[2:0]	**000**$_B$: Unknown when bit OP3 = 0 Unlimited when bit OP3 = 1 **001**$_B$: 700K **010**$_B$: 600K **011**$_B$: 500K **100**$_B$: 400K **101**$_B$: 300K **110**$_B$: 200K **111**$_B$: Reserved	1,2
Unlimited MAC		OP[3]	**0**$_B$: OP[2:0] define MAC Value **1**$_B$: Unlimited MAC Value	2,3
TRR mode BAn		OP[6:4]	**000**$_B$: Bank 0 **001**$_B$: Bank 1 **010**$_B$: Bank 2 **011**$_B$: Bank 3 **100**$_B$: Bank 4 **101**$_B$: Bank 5 **110**$_B$: Bank 6 **111**$_B$: Bank 7	
TRR mode		OP[7]	**0**$_B$: Disabled (Default) **1**$_B$: Enabled	

Note:
1. Unknown means that the device is not tested for tMAC and pass/fail values are unknown.
2. There is no restriction on the number of activates.
3. MR24 OP[2:0] is set to ZERO.

MR25 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0

Function	Register Type	Operand	Data	Note
PPR Resource	Read-only	OP[7:0]	**0**$_B$: PPR Resource is not available **1**$_B$: PPR Resource is available	

MR26-29 Register Information

Reserved for Future Use

MR30 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid 0 or 1							

Function	Register Type	Operand	Data	Note
SDRAM will ignore	Write-only	OP[7:0]	Don't' Care	1

Note:
1. This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

MR31 Register Information

Reserved for Future Use

MR32 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ Calibration Pattern "A" (Default = 5A$_H$)							

Function	Register Type	Operand	Data	Note
Return DQ Calibration Pattern MR32 + MR40	Write	OP[7:0]	**X**$_B$: An MPC command with OP[6:0]=100 0011$_B$ causes the device to return the DQ Calibration Pattern contained in this register and (followed by) the contents of MR40. A default pattern "5AH" is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the data pattern for a given DQ (See MR15 for more information)	1,2,3

MR33-38 Register Information

Reserved for Future Use

MR39 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid 0 or 1							

Function	Register Type	Operand	Data	Note
SDRAM will ignore	Write-only	OP[7:0]	Don't' Care	1

Note:
1. This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

MR40 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ Calibration Pattern "B" (Default = $3C_H$)							

Function	Register Type	Operand	Data	Note
Return DQ Calibration Pattern MR32 + MR40	Write-only	OP[7:0]	**X_B**: A default pattern "$3C_H$" is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register See MR32 for more information	1,2,3

Note:
1. The pattern contained in MR40 is concatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is initiated via a MPC command. The pattern transmitted serially on each data lane, organized "little endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27_H, then the first bit transmitted with be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111_B.
2. MR15 and MR20 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR22 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3 OP[6].
4. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3 OP[6].

MR41-47 Register Information

Do Not Use

MR48-50 Register Information

Reserved for Future Use

MR51 Register Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				Single-ended Clock	Single-ended WDQS	Single-ended RDQS	RFU

Function	Register Type	Operand	Data	Note
Single-ended RDQS	Write-only	OP[1]	0_B: Differential Read DQS (Default) 1_B: Single-ended Read DQS	1,2,3,4,5
Single-ended WDQS		OP[2]	0_B: Differential Write DQS (Default) 1_B: Single-ended Write DQS	1,2,3,4,6
Single-ended Clock		OP[3]	0_B: Differential Clock, CK_t/CK_c (Default) 1_B: Single-ended Clock, only CK_t	1,2,3,4,7

Note:
1. The features described in MR51 are optional. Please check the vendor for availability.
2. Device support for single ended mode features (MR51 OP[3:1]) is indicated in MR0 OP[5]
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
4. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.
5. When single-ended RDQS mode is enabled (MR51 OP[1] =1_B), DRAM drives Read DQSB low or Hi-Z.
6. When single-ended WDQS mode is enabled (MR51 OP[2] =1_B), Write DQSB is required to be at a valid logic level. A valid Write DQSB signal will meet this requirement.
7. When single ended Clock mode is enabled (MR51 OP[3] =1_B), CK_c is required to be the valid level required to be at a valid logic level. A valid CK_c signal will meet this requirement.

When DRAM is operating with single-ended mode, both CLKB and write DQSB shall be on "Low" state at all times whereas read DQSB is always on "Hi-Z" state. Refer to the table below.

		Differential mode	Single-ended mode
CLK	CLK	Valid	Valid
	CLKB	Valid	0
Write DQS	DQS	Valid	Valid
	DQSB	Valid	0
Read DQS	DQS	Valid	Valid
	DQSB	Valid	Hi-Z

MR52-63 Register Information

Reserved for Future Use

Truth Table

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR4x device must be reset or power-cycled and then restarted through the specified initialization sequence before normal operation can continue.

CKE signal has to be held High when the commands listed in the command truth table input.

SDRAM Command	SDR Command Pin	SDR CA Pin							Note
	CS	CA0	CA1	CA2	CA3	CA4	CA5	CK_t edge	
Deselect (DES)	L	X						R1	1,2
Multi-Purpose Command (MPC)	H	L	L	L	L	L	OP6	R1	1,9
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Precharge (PRE) (Per Bank, All Bank)	H	L	L	L	L	H	AB	R1	1,2,3,4
	L	BA0	BA1	BA2	V	V	V	R2	
Refresh (REF) (Per Bank, All Bank)	H	L	L	L	H	L	AB	R1	1,2,3,4
	L	BA0	BA1	BA2	V	V	V	R2	
Self Refresh Entry (SRE)	H	L	L	L	H	H	V	R1	1,2
	L	V						R2	
Write-1 (WR-1)	H	L	L	H	L	L	BL	R1	1,2,3,6, 7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
Self Refresh Exist (SRX)	H	L	L	H	L	H	V	R1	1,2
	L	V						R2	
Mask Write-1 (MWR-1)	H	L	L	H	H	L	L	R1	1,2,3,5, 6,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
RFU	H	L	L	H	H	H	V	R1	1,2
	L	V						R2	
Read (RD-1)	H	L	H	L	L	L	BL	R1	1,2,3,6, 7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
CAS-2 (Write-2, Mask Write-2, Read-2, MRR-2, MPC)	H	L	H	L	L	H	C8	R1	1,8,9
	L	C2	C3	C4	C5	C6	C7	R2	
RFU	H	L	H	L	H	L	V	R1	1,2
	L	V						R2	
RFU	H	L	H	L	H	H	V	R1	1,2
	L	V						R2	
Mode Register Write-1 (MRW-1)	H	L	H	H	L	L	OP7	R1	1,11
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
Mode Register Write-2 (MRW-2)	H	L	H	H	L	H	OP6	R1	1,11
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Mode Register Read-1 (MRR-1)	H	L	H	H	H	L	V	R1	1,2,12
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
RFU	H	L	H	H	H	H	V	R1	1,2
	L	V						R2	
Activate-1 (ACT-1)	H	H	L	R12	R13	R14	R15	R1	1,2,3,10
	L	BA0	BA1	BA2	V	R10	R11	R2	
Activate-2 (ACT-2)	H	H	H	R6	R7	R8	R9	R1	1,10
	L	R0	R1	R2	R3	R4	R5	R2	

Note:

1. All LPDDR4x commands except for Deselect are 2 clock cycle long and defined by states of CS and CA[5:0] at the first rising edge of clock. Deselect command is 1 clock cycle long.
2. "V" means "H" or "L" (a defined logic level). "X" means don't care in which case CA[5:0] can be floated.
3. Bank addresses BA[2:0] determine which bank is to be operated upon.
4. AB "HIGH" during Precharge or Refresh command indicates that command must be applied to all banks and bank address is a don't care.
5. Mask Write-1 command supports only BL 16. For Mark Write-1 command, CA5 must be driven LOW on first rising clock cycle (R1).

6. AP "HIGH" during Write-1, Mask Write-1 or Read-1 commands indicates that an auto-precharge will occur to the bank associated with the Write, Mask Write or Read command.
7. If Burst Length on-the-fly is enabled, BL "HIGH" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-Fly to BL=32. BL "LOW" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=16. If Burst Length on-the-fly is disabled, then BL must be driven to defined logic level "H" or "L".
8. For CAS-2 commands (Write-2 or Mask Write-2 or Read-2 or MRR-2 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration), C[1:0] are not transmitted on the CA[5:0] bus and are assumed to be zero. Note that for CAS-2 Write-2 or CAS-2 Mask Write-2 command, C[3:2] must be driven LOW.
9. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be immediately followed by CAS- 2 command consecutively without any other command in between. Write-1 or Mask Write-1 or Read-1 or mode register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be issued first before issuing CAS-2 command. MPC (Only Start & Stop DQS Oscillator, Start & Latch ZQ Calibration) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.
10. Activate-1 command must be immediately followed by Activate-2 command consecutively without any other command in between. Activate-1 command must be issued first before issuing Activate-2 command. Once Activate-1 command is issued, Activate-2 command must be issued before issuing another Activate-1 command.
11. MRW-1 command must be immediately followed by MRW-2 command consecutively without any other command in between. MRW-1 command must be issued first before issuing MRW-2 command.
12. MRR-1 command must be immediately followed by CAS-2 command consecutively without any other command in between. MRR-1 command must be issued first before issuing CAS-2 command.

CKE Truth Table

Device Current State	CKE_{n-1}	CKE_n	Command n	Operation	Device Next State	Note
Active Power Down	L	L	X	Maintain Active Power Down	Active Power Down	
	L	H	Deselect	Exit Active Power Down	Active	5,6
Idle Power Down	L	L	X	Main Idle Power Down	Idle Power Down	
	L	H	Deselect	Exit Idle Power Down	Idle	5,6
Self Refresh	L	L	X	Main Power-Down state within Self Refresh	Self Refresh	
	L	H	Deselect	Exit SREF Power-down, enable Command Decode	Self Refresh	5,6,7
	H	L	Deselect	Enter SREF Power-Down, disable Command Decode	Self Refresh	5,7
	H	H	See Note 7	See Note 7	Self Refresh	7
Bank(s) Active	H	L	Deselect	Enter Active Power Down	Active Power Down	5
All Banks Idle	H	L	Deselect	Enter Idle Power Down	Idle Power Down	5,8
Command Entry	H	H	Refer to the Command Truth Table			

Note:
1. CKE is a strictly asynchronous input, and as such, has no relationship to CK.
2. "X" means "don't care."
3. "Current State" is the state of the LPDDR4x prior to a toggle of CKE.
4. "CKE_{n-1}" is the logic state of CKE prior to a CKE toggle event, and "CKE_n" is the state of CKE after the toggle event.
5. "Deselect" is the only valid command that can be present on the bus when CKE is toggled.
6. Power-Down exit time (tXP) should elapse before a command other than Deselect is issued. The clock must toggle at least twice during the tXP period and must be stable before issuing a command.
7. When the device is in Self.Refresh, only MRR, MRW, or MPC commands are allowed. Certain restrictions apply to changing register contents via a MRW command during SREF. See MRW section for more information.
8. In the case of ODT disabled, all DQ output shall be Hi-Z. In the case of ODT enabled, all DQ shall be terminated to V_{SSQ}

State Truth Table

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all banks.

Current State Bank n, Command to Bank n

Current State	Command	Operation	Next State	Note
Any	NOP	Continuous pervious operation	Current State	
Idle	Activate	Select and Activate Row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refresh (All Bank)	7
	MRW	Write value to	MR Writing	7
	MRR	Read value from	Idle MR Reading	
	Precharge	Deactivate Row in Bank or Banks	Precharging	8,13
Row Active	Read	Select column, and start Read Burst	Reading	10
	Write	Select column, and start Write Burst	Writing	10
	MRR	Read value from	Active MR Reading	
	Precharge	Deactivate Row in Bank or Banks	Precharging	8
Reading	Read	Select column, and start new Read Burst	Reading	9,10
	Write	Select column, and start Write Burst	Writing	9,10,11
Writing	Write	Select column, and start new Write Burst	Writing	9,10
	Read	Select column, and start Read Burst	Reading	9,10,12

Note:

1. The table applies when both CKE_{n-1} and CKE_n are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State Definitions:
   - Idle: The bank or banks have been precharged, and tRP has been met.
   - Active: A row in the bank has been activated, and tRCD has been met. No data bursts / accesses and no register accesses are in progress.
   - Reading: A Read burst has been initiated, with Auto Precharge disabled.
   - Writing: A Write burst has been initiated, with Auto Precharge disabled.
4. The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and, and according to .
   - Precharging: starts with the registration of a Precharge command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
   - Row Activating: starts with registration of an Activate command and ends when tRCD is met. Once tRCD is met, the bank will be in the 'Active' state.
   - Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
   - Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.
   - Refreshing (Per Bank): starts with registration of a Refresh (Per Bank) command and ends when tRFCpb is met. Once tRFCpb is met, the bank will be in an 'idle' state.
   - Refreshing (All Bank): starts with registration of a Refresh (All Bank) command and ends when tRFCab is met. Once tRFCab is met, the device will be in an 'all banks idle' state.
   - Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
   - Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.
   - Idle MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
   - Active MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Active state.
   - Precharging All: starts with the registration of a Precharge-All command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
6. Bank-specific; requires that the bank is idle and no bursts are in progress.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
9. A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.
10. The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
11. A Write command may be applied after the completion of the Read burst; burst terminates are not permitted.
12. A Read command may be applied after the completion of the Write burst, burst terminates are not permitted.
13. If a Precharge command is issued to a bank in the Idle state, tRP shall still apply.

Current State Bank n, Command to Bank m

Current State Bank n	Command Bank m	Operation	Next State Bank m	Note
Any	NOP	Continuous pervious operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	
Row Activating, Active, or Precharging	Activate	Select and Activate Row in Bank m	Active	6
	Read	Select column, and start Read Burst from Bank m	Reading	7
	Write	Select column, and start Write Burst to Bank m	Writing	7
	Precharge	Deactivate Row in Bank or Banks	Precharging	8
	MRR	Read value from	Idle MR Reading or Active MR Reading	9,10
Reading (Autoprecharging disabled)	Read	Select column, and start Read Burst from Bank m	Reading	7
	Write	Select column, and start Write Burst to Bank m	Writing	7,12
	Active	Select and Activate Row in Bank m	Active	
	Precharge	Deactivate Row in Bank or Banks	Precharging	8
Writing/Masked Writing (Autoprecharging disabled)	Read	Select column, and start Read Burst from Bank m	Reading	7,14
	Write	Select column, and start Write Burst to Bank m	Writing	7
	Active	Select and Activate Row in Bank m	Active	
	Precharge	Deactivate Row in Bank or Banks	Precharging	8
Reading with Autoprecharging	Read	Select column, and start Read Burst from Bank m	Reading	7,13
	Write	Select column, and start Write Burst to Bank m	Writing	7,12,13
	Active	Select and Activate Row in Bank m	Active	
	Precharge	Deactivate Row in Bank or Banks	Precharging	8
Writing/Masked Writing with Autoprecharging	Read	Select column, and start Read Burst from Bank m	Reading	7,13,14
	Write	Select column, and start Write Burst to Bank m	Writing	7,13
	Active	Select and Activate Row in Bank m	Active	
	Precharge	Deactivate Row in Bank or Banks	Precharging	8

Note:

1. The table applies when both CKE_{n-1} and CKE_n are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State Definitions:
   - Idle: The bank has been precharged, and tRP has been met.
   - Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   - Reading: A Read burst has been initiated, with Auto Precharge disabled.
   - Writing: A Write burst has been initiated, with Auto Precharge disabled
4. Refresh, Self-Refresh, and Mode register Write commands may only be issued when all banks are idle.
5. The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:
   - Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
   - Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.
   - Idle MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
   - Active MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Active state.
6. tRRD must be met between Activate command to Bank n and a subsequent Activate command to Bank m. Additionally, in the case of multiple banks activated, tFAW must be satisfied.
7. Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.
8. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
9. MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when tRCD is met.)
10. MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when tRP is met.)
11. The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon tRCD and tRP respectively.
12. A Write command may be applied after the completion of the Read burst, burst terminates are not permitted.
13. Read with auto precharge enabled or a Write with Auto Precharge enabled may be followed by any valid command to other banks provided that the timing restrictions described in the Precharge & Auto Precharge clarification table are followed.
14. A Read command may be applied after the completion of the Write burst, burst terminates are not permitted.

Absolute Maximum DC Rating

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Parameter	Symbol	Min	Max	Unit	Note
V_{DD1} supply voltage relative to V_{SS}	V_{DD1}	-0.4	2.1	V	1
V_{DD2} supply voltage relative to V_{SS}	V_{DD2}	-0.4	1.5	V	1
V_{DDQ} supply voltage relative to V_{SSQ}	V_{DDQ}	-0.4	1.0	V	1
Voltage on any ball except V_{DD1} relative to V_{SS}	V_{IN}, V_{OUT}	-0.4	1.5	V	
Storage Temperature	T_{STG}	-55	125	℃	2

Note:

1. See Power Ramp for relationship between power supplies.
2. Storage Temperature is the case surface temperature on the center/top side of the LPDDR4x device. For the measurement conditions, please refer to JESD51-2 standard

AC & DC Operating Condition

Recommended DC Operating Condition

Symbol	DRAM	LPDDR4x			Unit	Note
		Min	Typ	Max		
V_{DD1}	Core 1 Power	1.70	1.80	1.95	V	1,2
V_{DD2}	Core 2 Power / Input Buffer Power	1.06	1.10	1.17	V	1,2,3
V_{DDQ}	O/I Buffer Power	0.57	0.60	0.65	V	2,3

Note:
1. V_{DD1} uses significantly less current than V_{DD2}.
2. The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
3. The voltage noise tolerance from DC to 20MHz exceeding a pk-pk tolerance of 45mv at the DRAM ball is not included in the TdIVW.

Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input Leakage Current	I_L	-2	2	uA	1,2

Note:
1. For CK_t, CK_c, CKE, CS, CA, ODT_CA and RESET_n. Any input 0V ≤ V_{IN} ≤ V_{DD2} (All other pins not under test = 0V)
2. CA ODT is disabled for CK_t, CK_c, CS and CA.

Input/Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/Output Leakage Current	I_{OZ}	-2.5	2.5	uA	1,2

Note:
1. For DQ, DQS_t, DQS_c and DMI. Any I/O 0V ≤ V_{OUT} ≤ V_{DDQ}
2. I/O status are disabled. High Impedance and ODT off.

Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit	Note
Commercial Temperature	T_{OPER}	-25	85	℃	1,2
Industrial Temperature		-40	95	℃	1,2

Note:
1. Operating Temperature is the case surface temperature on the center top side of the LPDDR4x device. For the measurement conditions, please refer to JESD51-2.
2. Either the device case temperature rating or the temperature sensor (See "Temperature Sensor" on [Command Definition & Timing Diagram]) may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the Commercial or Industrial Temperature Ranges. For example, T_{CASE} may be above 95℃ when the temperature sensor indicates a temperature of less than 95℃.

AC & DC Input Measurement Level

1.1 V High Speed LVCMOS (HS_LLVCMOS)

Standard Specification

All voltages are referenced to ground except where noted.

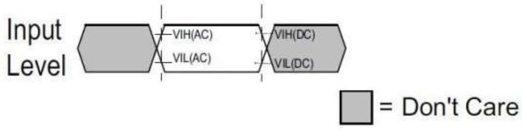
DC Electrical Characteristics

LPDDR4x Input Level for CKE

This definition applies to CKE_A/B.

Parameter	Symbol	Min	Max	Unit	Note
Input High Level (AC)	$V_{IH(AC)}$	0.75 x V_{DD2}	V_{DD2} + 0.2	V	1
Input Low Level (AC)	$V_{IL(AC)}$	-0.2	0.25 x V_{DD2}	V	1
Input High Level (DC)	$V_{IH(DC)}$	0.65 x V_{DD2}	V_{DD2} + 0.2	V	
Input Low Level (DC)	$V_{IL(DC)}$	-0.2	0.35 x V_{DD2}	V	

Note:



Refer to LPDDR4x AC Over/Undershoot section.

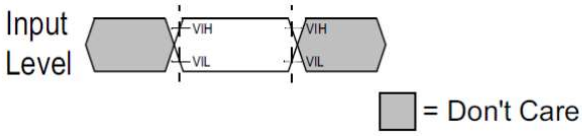
1. AC level is guaranteed transition point.
2. DC level is hysteresis.

LPDDR4x Input Level for RESET_n and ODT_CA

This definition applies to RESET_n and ODT_CA.

Parameter	Symbol	Min	Max	Unit	Note
Input High Level	V_{IH}	0.80 x V_{DD2}	V_{DD2} + 0.2	V	1
Input Low Level	V_{IL}	-0.2	0.20 x V_{DD2}	V	1

Note:

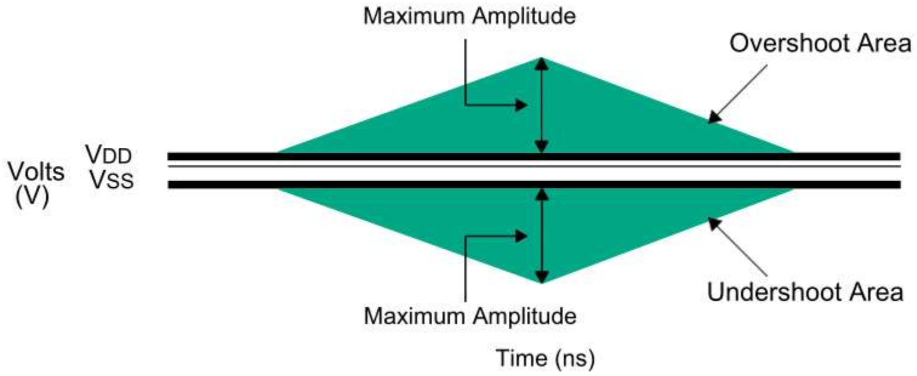


Refer to LPDDR4x AC Over/Undershoot section.

AC Over/Undershoot

LPDDR4x AC Over/Undershoot

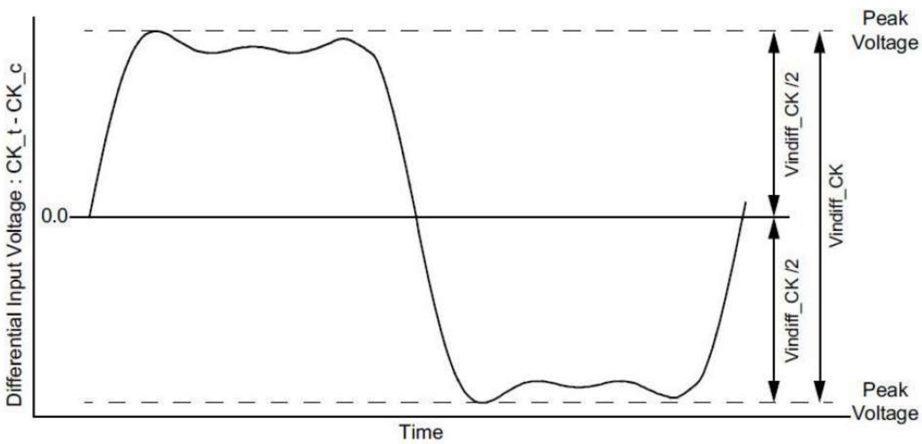
Parameter	Value	Unit
Maximum Peak Amplitude allowed for Overshoot area	0.35	V
Maximum Peak Amplitude allowed for Undershoot area	0.35	V
Maximum Overshoot area above V_{DD} / V_{DDQ}	0.80	V
Maximum Undershoot area above V_{SS} / V_{SSQ}	0.80	V



Differential Input Voltage

Differential Input Voltage for CK

The minimum input voltage needs to satisfy both V_{INdiff_CK} and V_{INdiff_CK} /2 specification at input receiver and their measurement period is 1tCK. V_{INdiff_CK} is the peak-to-peak voltage centered on 0 volts differential and V_{INdiff_CK} /2 is max and min peak voltage from 0V.



Parameter	Symbol	Data Rate		Unit	Note
		4266			
		Min	Max		
CK Differential Input Voltage	V_{INdiff_CK}	360	-	mV	1

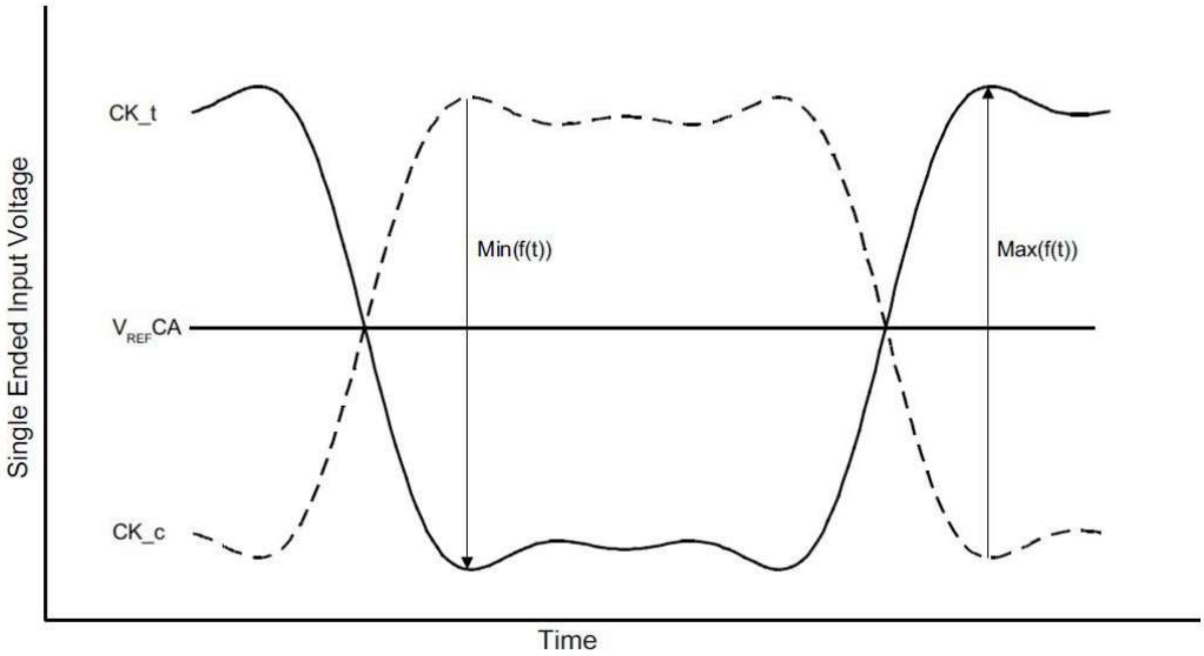
Note:

1. The peak voltage of Differential CK signals is calculated in the following equation.
   V_{INdiff_CK} = (Max Peak Voltage) - (Min Peak Voltage)
   - Max Peak Voltage = Max(f(t))
   - Min Peak Voltage = Min(f(t))
   - f(t) = $V_{CK\_t} - V_{CK\_c}$

Peak Voltage Calculation Method

The peak voltage of Differential Clock signals is calculated in the following equation.

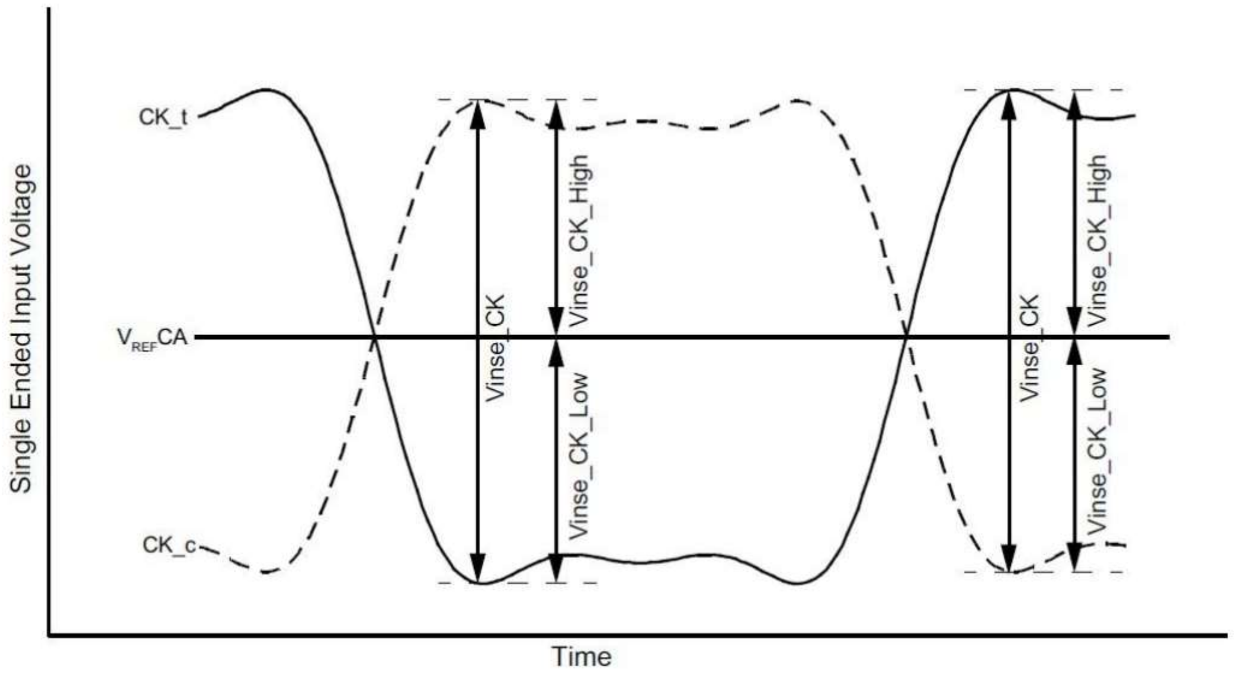
$V_{IHdiff.Peak}$ Voltage = Max(f(t))
$V_{ILdiff.Peak}$ Voltage = Min(f(t))
f(t) = V_{CK_t} - V_{CK_c}



Note:
1. V_{REFCA} is LPDDR4x internal setting value by V_{REF} Training.

Single-ended Input Voltage for Clock

The minimum input voltage needs to satisfy both V_{INse_CK}, $V_{INse\_CK\_High}$ / $V_{INse\_CK\_Low}$ specification at input receiver.



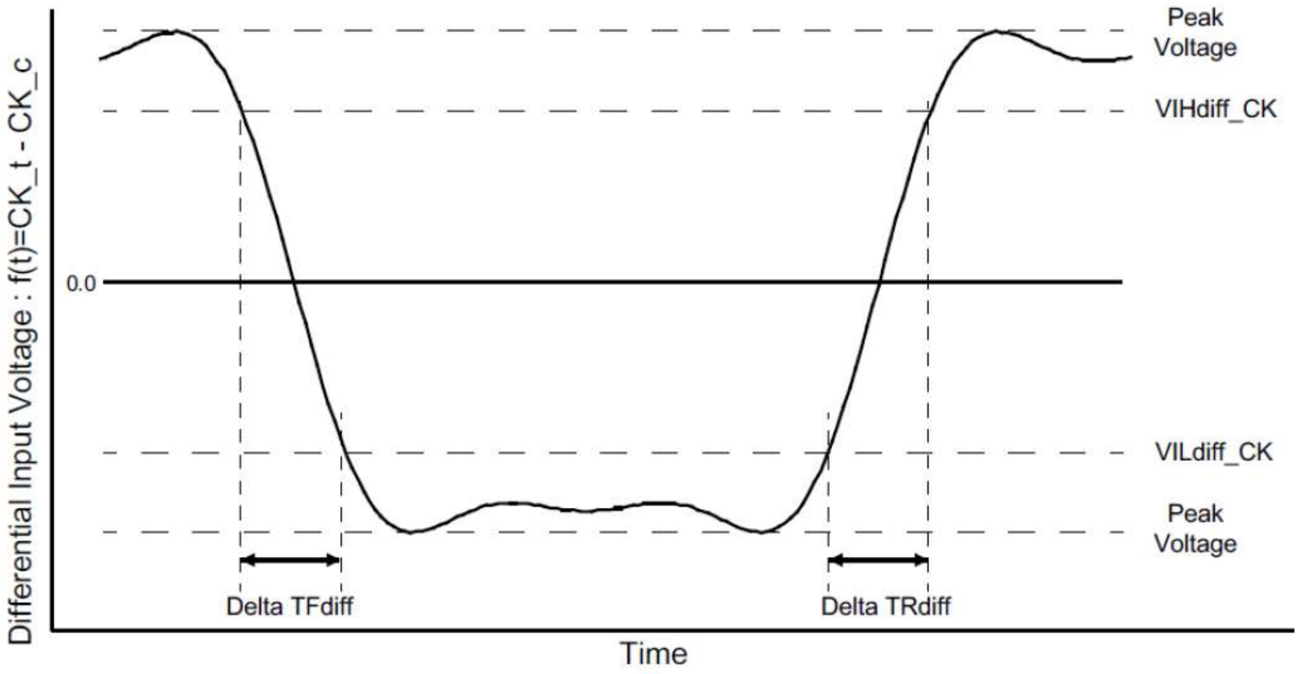
Note:

1. V_{REFCA} is LPDDR4x internal setting value by V_{REF} Training.

Parameter	Symbol	Date Rate		Unit
		4266		
		Min	Max	
Clock Single-Ended Input Voltage	V_{INse_CK}	180	-	mV
Clock Single-Ended Input Voltage High for V_{REFDQ}	$V_{INse\_CK\_High}$	90	-	mV
Clock Single-Ended Input Voltage Low for V_{REFDQ}	$V_{INse\_CK\_Low}$	90	-	mV

Differential Input Slew Rate Definition for Clock

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in figure and the following Tables.



Note:
1. Differential signal rising edge from V_{ILdiff_CK} to V_{IHdiff_CK} must be monotonic slope.
2. Differential signal falling edge from V_{IHdiff_CK} to V_{ILdiff_CK} must be monotonic slope.

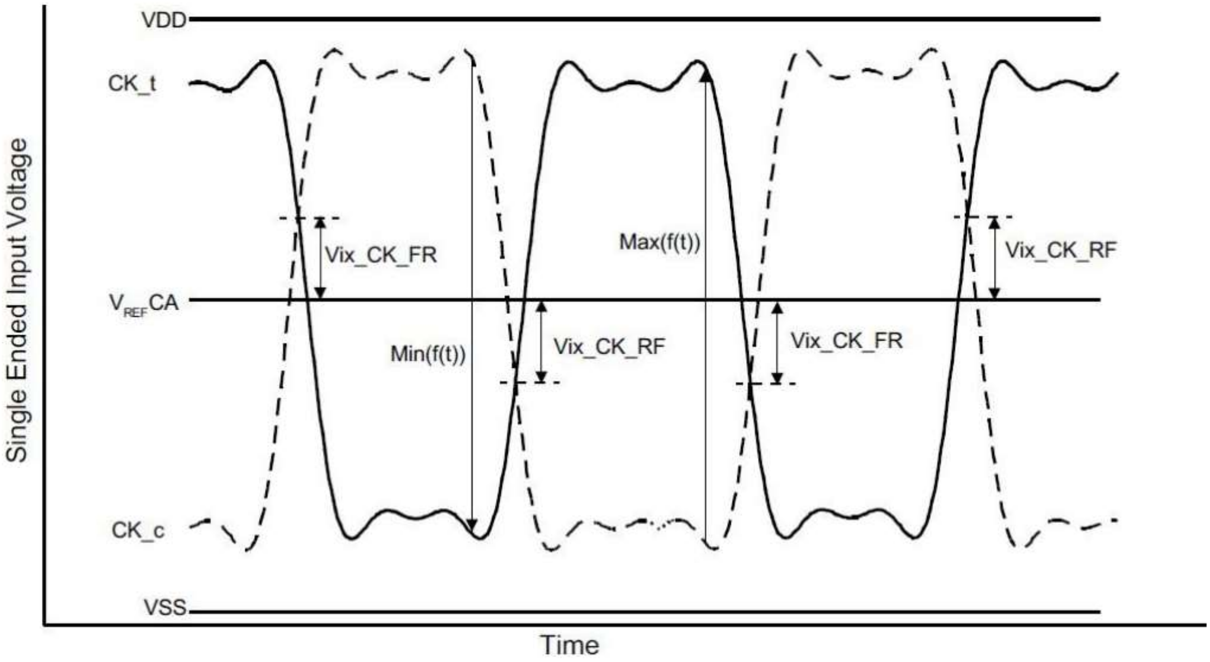
Description	From	To	Defined by
Differential Input Slew Rate for Rising Edge (CK_t – CK_c)	V_{ILdiff_CK}	V_{IHdiff_CK}	$\|V_{ILdiff\_CK} – V_{IHdiff\_CK}\|$ / Delta TRdiff
Differential Input Slew Rate for Falling Edge (CK_t – CK_c)	V_{IHdiff_CK}	V_{ILdiff_CK}	$\|V_{ILdiff\_CK} – V_{IHdiff\_CK}\|$ / Delta TFdiff

Parameter	Symbol	Date Rate		Unit
		4266		
		Min	Max	
Differential Input High	V_{ILdiff_CK}	145	-	mV
Differential Input Low	V_{IHdiff_CK}	-	-145	mV

Parameter	Symbol	Date Rate		Unit
		4266		
		Min	Max	
Differential Input Slew Rate for Clock	SRIdiff_CK	2	14	V/ns

Differential Input Cross Point Voltage for Clock

The cross-point voltage of differential input signals (CK_t, CK_c) must meet the requirements in the table below. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the mid-level that is V_{REFCA}.



Parameter	Symbol	Date Rate		Unit	Note
		4266			
		Min	Max		
Clock Differential Input Cross Point Voltage Ratio	$V_{IX\_CK\_ratio}$	-	25	%	1,2

Note:
1. $V_{IX\_CK\_Ratio}$ is defined by this equation: $V_{IX\_CK\_Ratio} = V_{IX\_CK\_FR}/|Min(f(t))|$
2. $V_{IX\_CK\_Ratio}$ is defined by this equation: $V_{IX\_CK\_Ratio} = V_{IX\_CK\_RF}/Max(f(t))$

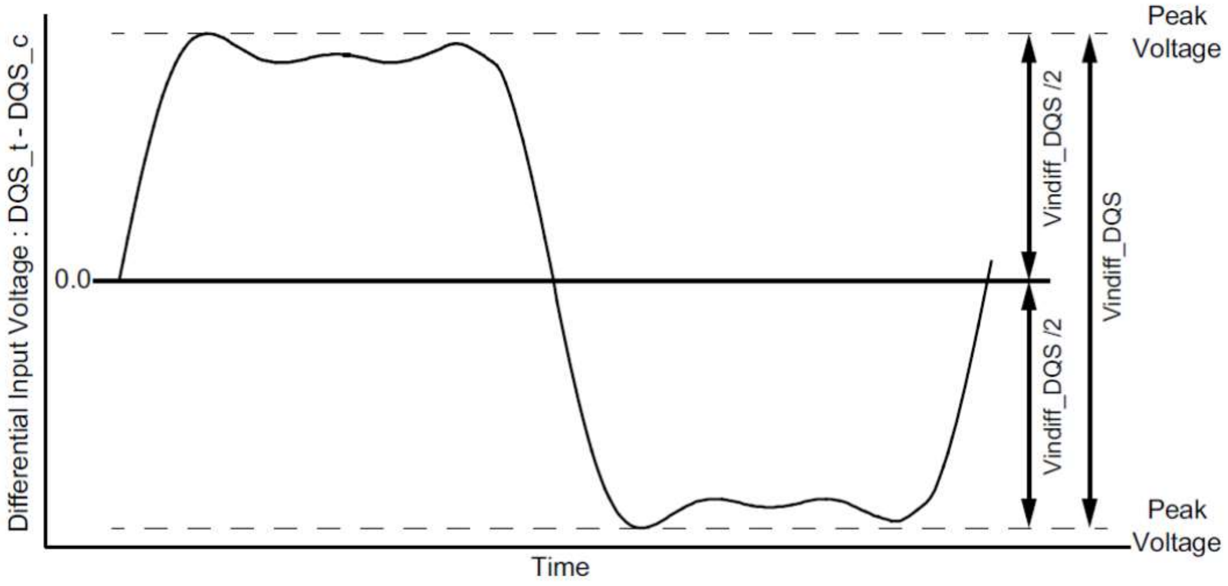
AC/DC Input Level for ODT Input

Description	Symbol	Min	Max	Unit	Note
ODT Input High Level (AC)	$V_{IHODT(AC)}$	0.75 x V_{DD}	V_{DD} + 0.2	V	1
ODT Input Low Level (AC)	$V_{ILODT(AC)}$	-0.2	0.25 x V_{DD}	V	1
ODT Input High Level (DC)	$V_{IHODT(DC)}$	0.65 x V_{DD}	V_{DD} + 0.2	V	
ODT Input Low Level (DC)	$V_{ILODT(DC)}$	-0.2	0.35 x V_{DD}	V	

Note:
1. See Overshoot and Undershoot Specification.

Differential Input Voltage for DQS

The minimum input voltage need to satisfy both V_{INdiff_DQS} and V_{INdiff_DQS} /2 specification at input receiver and their measurement period is 1UI(tCK/ 2). V_{INdiff_DQS} is the peak-to-peak voltage centered on 0 volts differential and V_{INdiff_DQS} /2 is max and min peak voltage from 0V.



Parameter	Symbol	Date Rate 4266 Min	Date Rate 4266 Max	Unit	Note
DQS Differential Input	V_{INdiff_DQS}	340	-	mV	1

Note:

1. The peak voltage of Differential DQS signals is calculated in the following equation.
   V_{INdiff_DQS} = (Max Peak Voltage) - (Min Peak Voltage)
   - Max Peak Voltage = Max(f(t))
   - Min Peak Voltage = Min(f(t))
   - f(t) = V_{DQS_t} - V_{DQS_c}

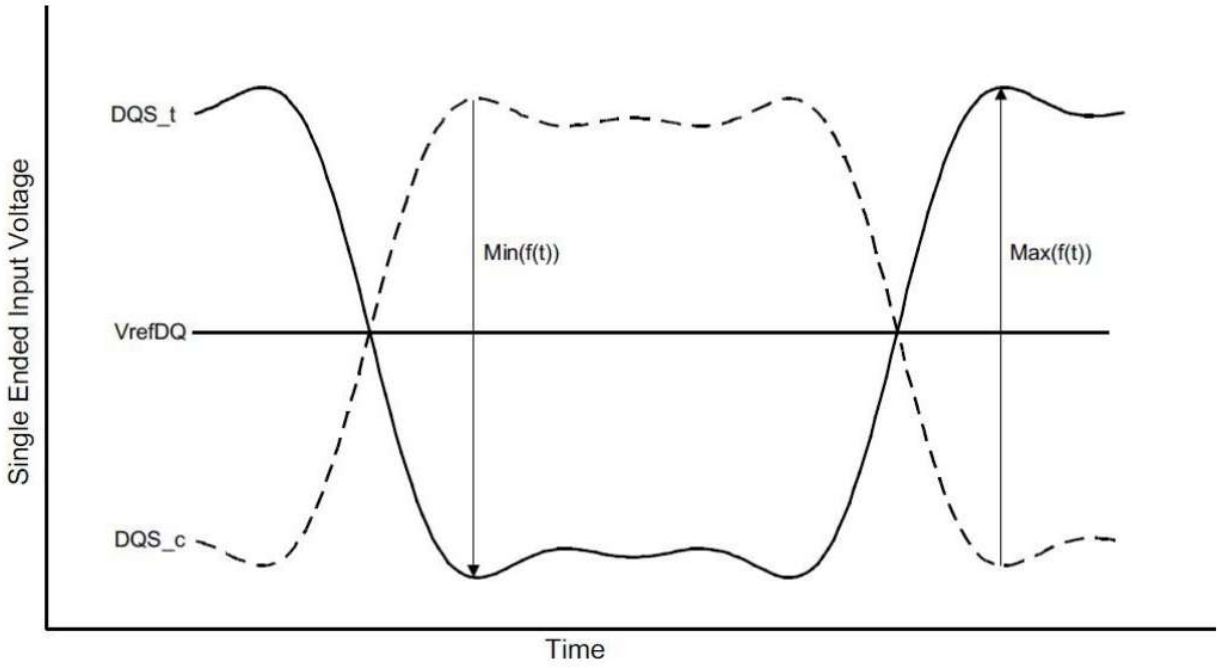
Peak Voltage Calculation Method

The peak voltage of Differential DQS signals is calculated in the following equation.

$V_{IHdiff.Peak}$ Voltage = Max(f(t))

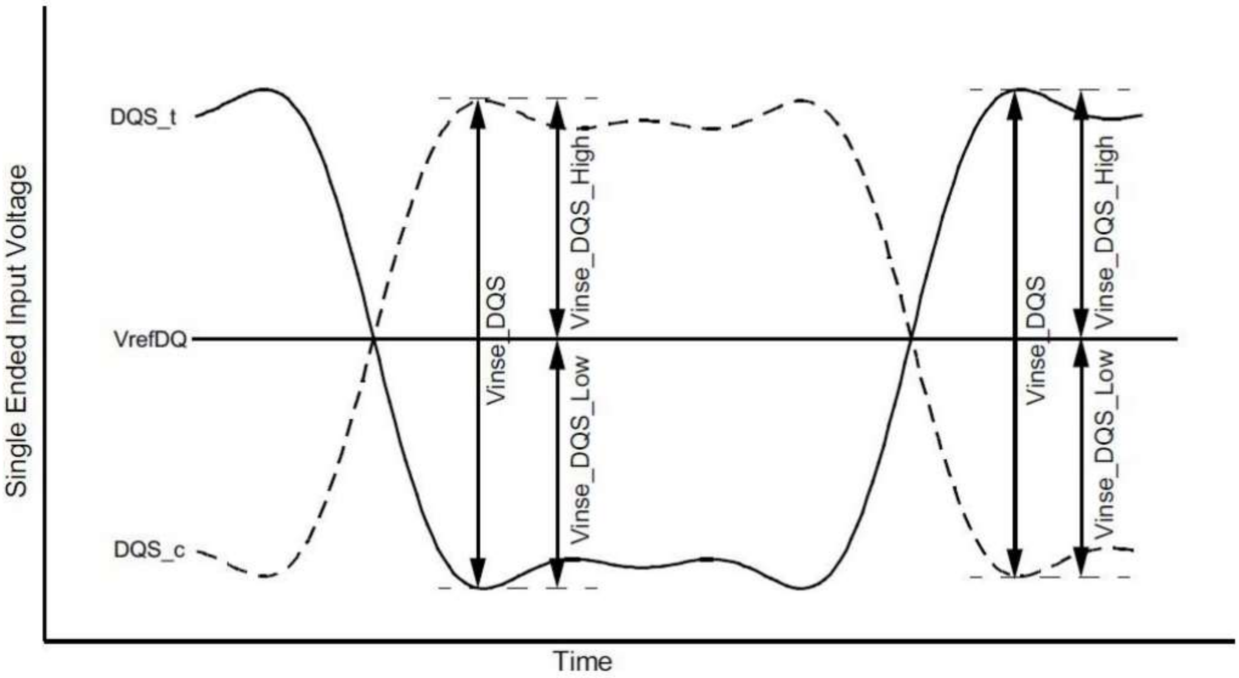
$V_{ILdiff.Peak}$ Voltage = Min(f(t))

f(t) = V_{DQS_t} - V_{DQS_c}



Single-ended Input Voltage for DQS

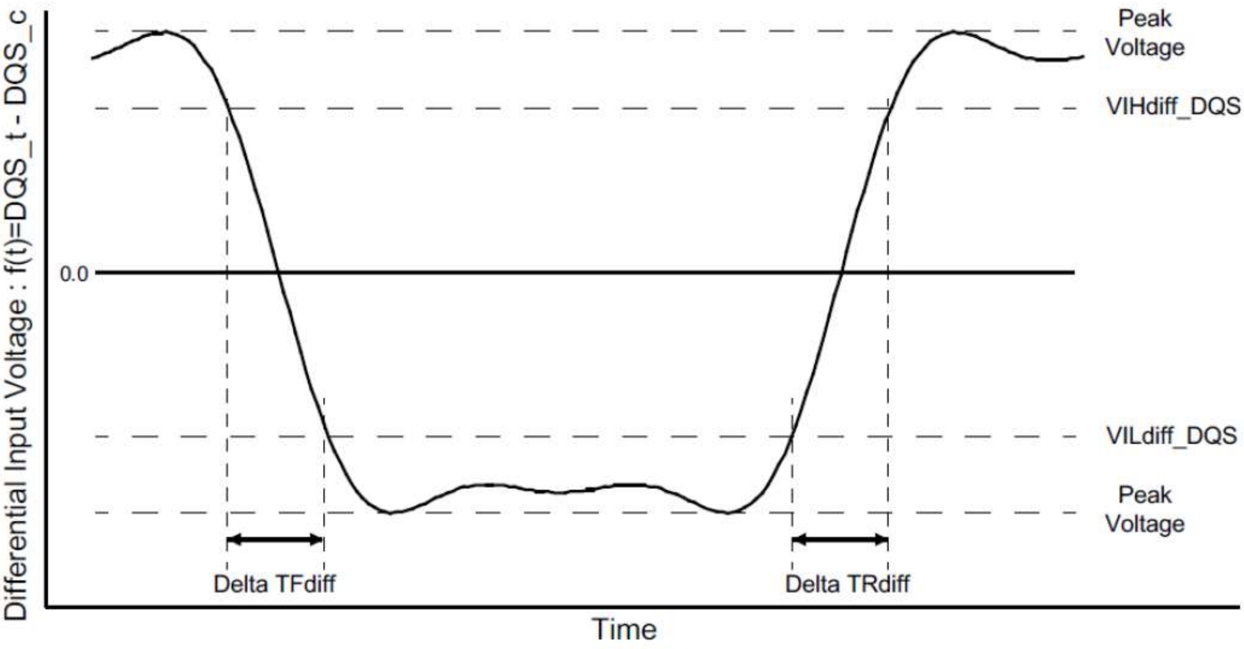
The minimum input voltage needs to satisfy both V_{INse_DQS}, $V_{INse\_DQS\_High}$ / $V_{INse\_DQS\_Low}$ specification at input receiver.



Parameter	Symbol	Date Rate 4266		Unit	Note
		Min	Max		
DQS Single-ended Input Voltage	V_{INse_DQS}	170	-	mV	
DQS Single-ended Input Voltage High from V_{REFDQ}	$V_{INse\_DQS\_High}$	85	-	mV	
DQS Single-ended Input Voltage Low from V_{REFDQ}	$V_{INse\_DQS\_Low}$	85	-	mV	

Differential Input Slew Rate Definition for DQS

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in figure and table



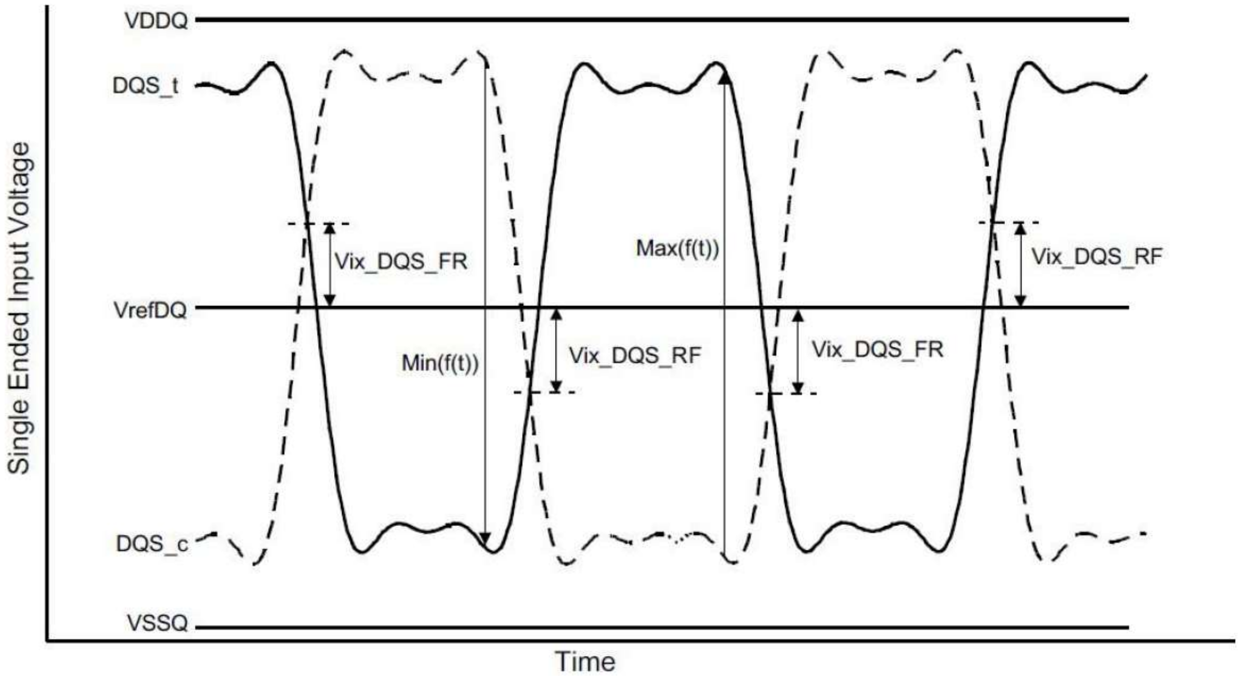
Description	From	To	Defined by
Differential Input Slew Rate for Rising Edge (DQS_t - DQS_c)	V_{ILdiff_DQS}	V_{IHdiff_DQS}	$\|V_{ILdiff\_DQS} - V_{IHdiff\_DQS}\|$ / Delta TRdiff
Differential Input Slew Rate for Falling Edge (DQS_t – DQS_c)	V_{IHdiff_DQS}	V_{ILdiff_DQS}	$\|V_{ILdiff\_DQS} - V_{IHdiff\_DQS}\|$ / Delta TFdiff

Parameter	**Symbol**	**Date Rate**		**Unit**
		4266		
		Min	**Max**	
Differential Input High	V_{IHdiff_DQS}	120	-	mV
Differential Input Low	V_{ILdiff_DQS}	-	-120	mV

Parameter	**Symbol**	**Date Rate**		**Unit**
		4266		
		Min	**Max**	
Differential Input Slew Rate	SRIdiff	2	14	V/ns

Differential Input Cross Point Voltage for DQS

The cross-point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in table. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the mid-level that is V_{REFDQ}

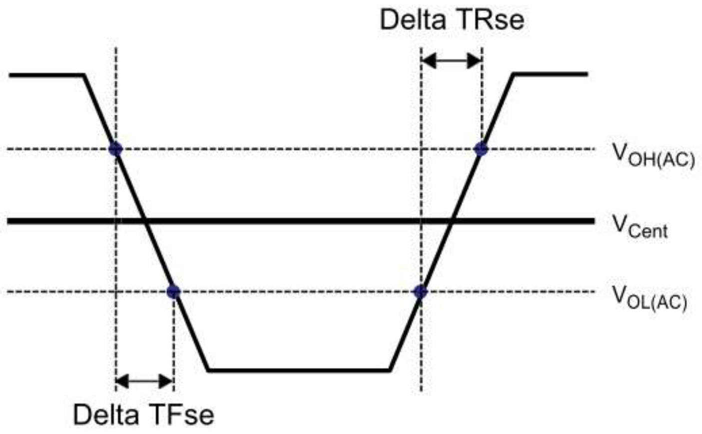


Parameter	Symbol	Date Rate		Unit	Note
		4266			
		Min	Max		
Clock Differential Input Cross Point Voltage Ratio	$V_{IX\_CK\_ratio}$	-	20	%	1,2

Note:

1. $V_{IX\_DQS\_Ratio}$ is defined by this equation: $V_{IX\_DQS\_Ratio} = V_{IX\_DQS\_FR}/|Min(f(t))|$
2. $V_{IX\_DQS\_Ratio}$ is defined by this equation: $V_{IX\_DQS\_Ratio} = V_{IX\_DQS\_RF}/Max(f(t))$

Single Ended Output Slew Rate



Parameter	Symbol	Value		Unit
		Min	Max	
Single-ended Output Slew Rate ($V_{OH} = V_{DDQ}$ x 0.5)	SRQse	3.0	9.0	V/ns
Output Slew-Rate matching Ratio (Rise to Fall)		0.8	1.2	

Description:

SR: Slew Rate

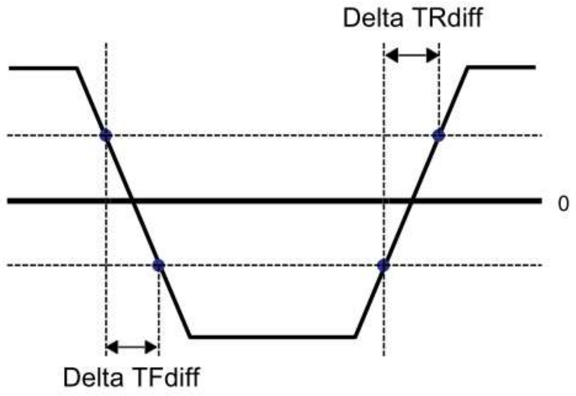
Q = Query Output (like in DQ, which stands for Data-in, Query-Output)

se = Single-ended Signals

Note:

1. Measured with output reference load.
2. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)} = 0.2 \times V_{OH(DC)}$ and $V_{OH(AC)} = 0.8 \times V_{OH(DC)}$.
4. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

Differential Output Slew Rate



Parameter	Symbol	Value		Unit
		Min	Max	
Differential Output Slew Rate (V_{OH} = V_{DDQ} x 0.5)	S_{RQdiff}	6.0	18.0	V/ns

Description:

SR: Slew Rate

Q = Query Output (like in DQ, which stands for Data-in, Query-Output)

diff = Differential signal

Note:

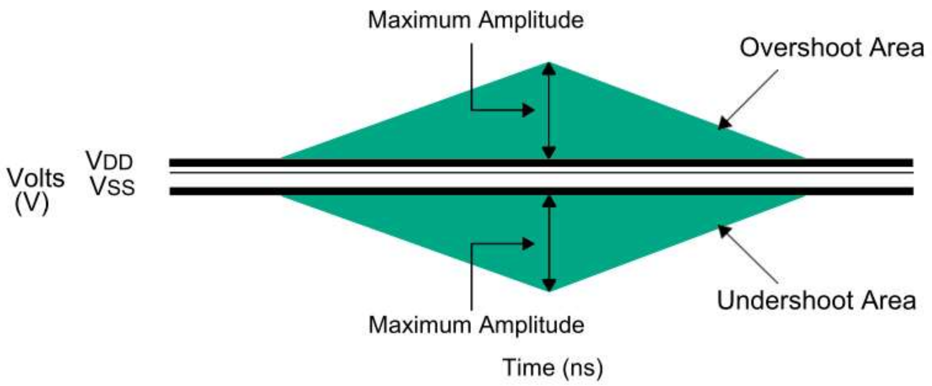
1. Measured with output reference load.
2. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$=-0.8×$V_{OH(DC)}$ and $V_{OH(AC)}$=0.8×$V_{OH(DC)}$.
3. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

Overshoot and Undershoot for LVSTL

Parameter		Data Rate 4266	Unit
Maximum Peak Amplitude for Overshoot Area (see below figure)	Max	TBD	V
Maximum Peak Amplitude for Undershoot Area (see below figure)	Max	TBD	V
Maximum Overshoot Area above V_{DD} (see below figure)	Max	TBD	V-ns
Maximum Undershoot Area below V_{SS} (see below figure)	Max	TBD	V-ns

Note:

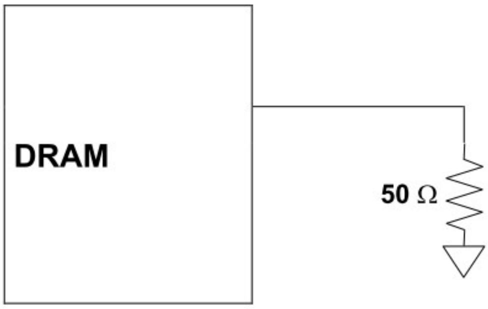
1. V_{DD2} stands for V_{DD} for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. V_{DD} stands for V_{DDQ} for DQ, DMI, DQS_t and DQS_c.
2. V_{SS} stands for V_{SS} for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. V_{SS} stands for V_{SSQ} for DQ, DMI, DQS_t and DQS_c.
3. Maximum peak amplitude values are referenced from actual V_{DD} and V_{SS} values.
4. Maximum area values are referenced from maximum operating V_{DD} and V_{SS} values.



Output Buffer Characteristics

LPDDR4x Driver Output Timing Reference Load

These ‘Timing Reference Loads’ are not intended as a precise representation of any particular system environment or a depiction of the actual load present by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics

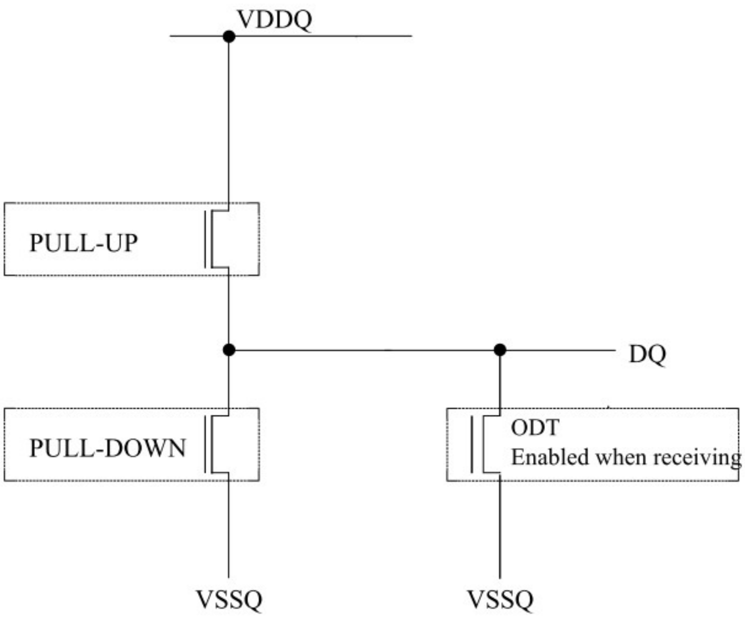


Note:

1. All output timing parameter values are reported with respect to this reference load. This reference load is also used to report slew rate.

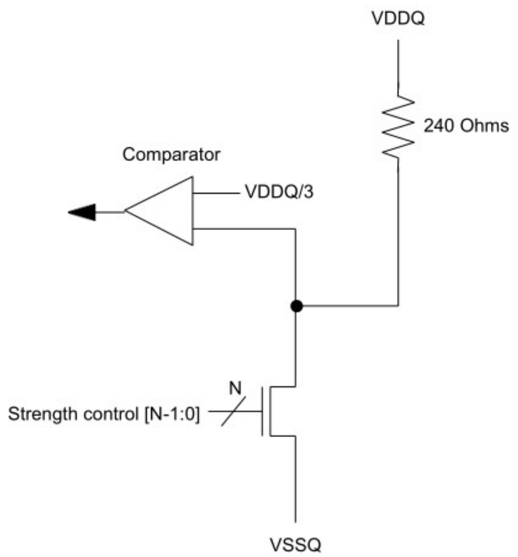
LVSTL (Low Voltage Swing Terminated Logic) I/O System

LVSTL I/O cell is comprised of pull-up, pull-down driver and a terminator. The basic cell is shown in the figure.

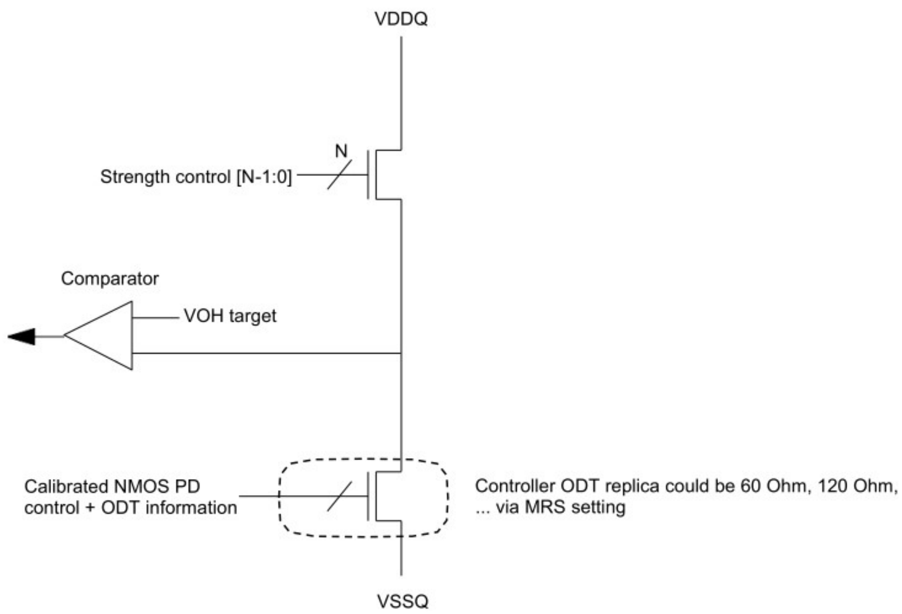


To ensure that the target impedance is achieved the LVSTL I/O cell is designed to calibrate as below procedure.

1. First calibrate the pull-down device against a 240ohm resister to V_{DDQ} via the ZQ pin.
   Set Strength Control to minimum setting
   Increase drive strength until comparator detects data bit is less than V_{DDQ} /2.
   NMOS pull-down device is calibrated to 240ohs



2. Then calibrate the pull-up device against the calibrated pull-down device.
   Set V_{OH} target and NMOS controller ODT replica via MRS (V_{OH} can be automatically controlled by ODT MRS)
   Set Strength Control to minimum setting
   Increase drive strength until comparator detects data bit is greater than V_{OH} target
   NMOS pull-up device is now calibrated to V_{OH} target



Input/Output Capacitance

Parameter	Symbol	Min	Max	Unit	Note
Input Capacitance, CK_t and CK_c	CCK	0.5	0.9	pF	1,2
Input Capacitance delta, CK_t and CK_c	CDCK	0	0.09	pF	1,2,3
Input Capacitance, all other input-only pins	CI	0.5	0.9	pF	1,2,4
Input Capacitance delta, all other input-only pins	CDI	-0.1	0.1	pF	1,2,5
Input/Output Capacitance, DQ, DMI, DQS_t and DQS_c	CIO	0.7	1.3	pF	1,2,6
Input/Output Capacitance delta, DQS_t and DQS_c	CDDQS	0	0.1	pF	1,2,7
Input/Output Capacitance delta, DQ and DMI	CDIO	-0.1	0.1	pF	1,2,8
Input/Output Capacitance, ZQ pin	CZQ	0	0.5	pF	1,2

Note:

1. This parameter applies to both die and package.
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (V_{NA}) with V_{DD1}, V_{DD2}, V_{DDQ}, V_{SS}, V_{SSQ} applied and all other pins floating.
3. Absolute value of CCK_t - CCK_c.
4. CI applies to CS_n, CKE, CA0-CA5.
5. CDI = CI - 0.5 × (CCK_t + CCK_c)
6. DMI loading matches DQ and DQS.
7. Absolute value of CDQS_t and CDQS_c.
8. CDIO = CIO - 0.5 × (CDQS_t + CDQS_c) in byte-lane.

IDD Specification Parameter and Test Condition

IDD Measurement Condition

The following definitions are used within the IDD measurement tables unless stated otherwise:

LOW: $V_{IN} \leq V_{IL(DC)}$ MAX
HIGH: $V_{IN} \geq V_{IH(DC)}$ MIN
STABLE: Inputs are stable at a HIGH or LOW level
SWITCHING: See Table for Differential Voltage for DQS

Switching for CA

CK_t edge	R1	R2	R3	R4	R5	R6	R7	R8
CKE	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
CS	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Note:
1. CS must always be driven LOW.
2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

CA Pattern for IDD4R for BL=16

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		H	H	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

Note:
1. BA[2:0] = 010_B, CA[9:4] = 000000_B or 111111_B, Burst Order CA[3:2] = 00_B or 11_B (Same as LPDDR3 IDD4R Spec)
2. Difference from LPDDR3 Spec: CA pins are kept low with DES CMD to reduce ODT current.

CA Pattern for IDD4W for BL=16

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		L	L	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

Note:

1. BA[2:0] = 010_B, CA[9:4] = 000000_B or 111111_B (Same as LPDDR3 IDD4W Spec.)
2. Difference from LPDDR3 Spec:
   1. No burst ordering
   2. CA pins are kept low with DES CMD to reduce ODT current

Data Pattern for IDD4W (DBI off) for BL=16

	DBI OFF Case									No of 1's
	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	16	16	16	16	16	16	16	16	16	

Note:

1. Simplified pattern compared with last showing.
   Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

Data Pattern for IDD4R (DBI off) for BL=16

	DBI OFF Case									No of 1's
	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	1	1	0	8
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	1	1	1	1	1	1	0	0	0	6
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	1	1	0	8
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	1	1	1	1	1	1	0	0	0	6
BL31	1	1	1	1	0	0	0	0	0	4
No. of 1's	16	16	16	16	16	16	16	16	16	

Note:

1. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

Data Pattern for IDD4W (DBI on) for BL=16

	DBI ON Case									No of 1's
	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	16	16	16	16	16	16	16	16	16	

DBI enabled burst

Data Pattern for IDD4R (DBI on) for BL=16

	DBI ON Case									No of 1's
	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	0	0	1	1
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	1	3
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	0	0	1	1
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	0	0	0	0	0	0	1	1	1	3
BL31	1	1	1	1	0	0	0	0	0	4
No. of 1's	16	16	16	16	16	16	16	16	16	

DBI enabled burst

IDD Specification

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire elevated temperature range.

Parameter / Condition	Symbol	Power Supply	Note

Operating one bank Active-Precharge Current:
tCK = tCKmin;
tRC = tRCmin;
CKE is HIGH;
CS is LOW between valid commands;
CA bus inputs are switching
Data bus inputs are stable;
ODT is disabled
	$IDD0_1$	V_{DD1}	1,10

	$IDD0_2$	V_{DD2}	1,10
	$IDD0_Q$	V_{DDQ}	1,3,10
Idle Power-Down Standby Current: tCK = tCKmin; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	$IDD2P_1$	V_{DD1}	1,10
	$IDD2P_2$	V_{DD2}	1,10
	$IDD2P_Q$	V_{DDQ}	1,3,10
Idle Power-Down Standby Current with Clock stop: CK_t =LOW, CK_c =HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	$IDD2PS_1$	V_{DD1}	1,10
	$IDD2PS_2$	V_{DD2}	1,10
	$IDD2PS_Q$	V_{DDQ}	1,3,10
Idle non Power-Down Standby Current: tCK = tCKmin; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	$IDD2N_1$	V_{DD1}	1,10
	$IDD2N_2$	V_{DD2}	1,10
	$IDD2N_Q$	V_{DDQ}	1,3,10
Idle non Power-Down Standby Current with Clock stopped: CK_t=LOW; CK_c=HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	$IDD2NS_1$	V_{DD1}	1,10
	$IDD2NS_2$	V_{DD2}	1,10
	$IDD2NS_Q$	V_{DDQ}	1,3,10
Active Power-Down Standby Current: tCK = tCKmin; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	$IDD3P_1$	V_{DD1}	1,10
	$IDD3P_2$	V_{DD2}	1,10
	$IDD3P_Q$	V_{DDQ}	1,3,10
Active Power-Down Standby Current with Clock stop: CK_t=LOW, CK_c=HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	$IDD3PS_1$	V_{DD1}	1,10
	$IDD3PS_2$	V_{DD2}	1,10
	$IDD3PS_Q$	V_{DDQ}	1,4,10

Parameter / Condition	Symbol	Power Supply	Note
Active non Power-Down Standby Current: tCK = tCKmin; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	$IDD3N_1$	V_{DD1}	1,10
	$IDD3N_2$	V_{DD2}	1,10
	$IDD3N_Q$	V_{DDQ}	1,4,10
Active non Power-Down Standby Current with Clock stopped: CK_t=LOW, CK_c=HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	$IDD3NS_1$	V_{DD1}	1,10
	$IDD3NS_2$	V_{DD2}	1,10
	$IDD3NS_Q$	V_{DDQ}	1,4,10
Operating Burst READ Current: tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer ODT is disabled	$IDD4R_1$	V_{DD1}	1,10
	$IDD4R_2$	V_{DD2}	1,10
	$IDD4R_Q$	V_{DDQ}	1,5,10
Operating Burst WRITE Current: tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT is disabled	$IDD4W_1$	V_{DD1}	1,10
	$IDD4W_2$	V_{DD2}	1,10
	$IDD4W_Q$	V_{DDQ}	1,4,10

All-bank REFRESH Burst Current:
tCK = tCKmin;
CKE is HIGH between valid commands;
tRC = tRFCabmin;
Burst refresh;
CA bus inputs are switching;
Data bus inputs are stable;
ODT is disabled
	$IDD5_1$	V_{DD1}	1,10

	$IDD5_2$	V_{DD2}	1,10
	$IDD5_Q$	V_{DDQ}	1,4,10

All-bank REFRESH Average Current:
tCK = tCKmin;
CKE is HIGH between valid commands;
tRC = tREFI;
CA bus inputs are switching;
Data bus inputs are stable;
ODT is disabled
	$IDD5AB_1$	V_{DD1}	1,10

	$IDD5AB_2$	V_{DD2}	1,10
	$IDD5AB_Q$	V_{DDQ}	1,4,10

Per-bank REFRESH Average Current:
tCK = tCKmin;
CKE is HIGH between valid commands;
tRC = tREFI/8;
CA bus inputs are switching;
Data bus inputs are stable;
ODT is disabled
	$IDD5PB_1$	V_{DD1}	1,10

	$IDD5PB_2$	V_{DD2}	1,10
	$IDD5PB_Q$	V_{DDQ}	1,4,10
Power Down Self refresh current (-40°C to +95°C): CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are stable Data bus inputs are stable; Maximum 1x Self-Refresh Rate; ODT is disabled	$IDD6_1$	V_{DD1}	6,7,9,10
	$IDD6_2$	V_{DD2}	6,7,9,10
	$IDD6_Q$	V_{DDQ}	4,6,7,9,10

Note:

1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled: MR11[2:0] = 000_B.
3. IDD current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of V_{DDQ} and V_{DD2}.
5. Guaranteed by design with output load = 5pF and RON = 40ohm.
6. The 1x Self-Refresh Rate is the rate at which the LPDDR4x device is refreshed internally during Self-Refresh, before going into the elevated Temperature range.
7. This is the general definition that applies to full array Self Refresh.
8. For all IDD measurements, V_{IHCKE} = 0.8 x V_{DD2}, V_{ILCKE} = 0.2 x V_{DD2}.
9. IDD6 25°C is guaranteed, IDD6 95°C is typical of the distribution of the arithmetic mean.
10. These specification values are the summation of all the channel current and both channels are under the same condition at the same time.
11. Dual Channel devices are specified in dual channel operation (both channels operating together).

Symbol			Power Supply	4Gb x16 (1Ch, x16/Ch) 4266	Unit
IDD0	$IDD0_1$		V_{DD1}	5	mA
	$IDD0_2$		V_{DD2}	34	mA
	$IDD0_Q$		V_{DDQ}	0.25	mA
IDD2P	$IDD2P_1$		V_{DD1}	0.6	mA
	$IDD2P_2$		V_{DD2}	2.25	mA
	$IDD2P_Q$		V_{DDQ}	0.25	mA
IDD2PS	$IDD2PS_1$		V_{DD1}	0.6	mA
	$IDD2PS_2$		V_{DD2}	2.25	mA
	$IDD2PS_Q$		V_{DDQ}	0.25	mA
IDD2N	$IDD2N_1$		V_{DD1}	1.5	mA
	$IDD2N_2$		V_{DD2}	14.25	mA
	$IDD2N_Q$		V_{DDQ}	0.25	mA
IDD2NS	$IDD2NS_1$		V_{DD1}	1.5	mA
	$IDD2NS_2$		V_{DD2}	11	mA
	$IDD2NS_Q$		V_{DDQ}	0.25	mA
IDD3P	$IDD3P_1$		V_{DD1}	1.4	mA
	$IDD3P_2$		V_{DD2}	6.75	mA
	$IDD3P_Q$		V_{DDQ}	0.25	mA
IDD3PS	$IDD3PS_1$		V_{DD1}	1.4	mA
	$IDD3PS_2$		V_{DD2}	6.75	mA
	$IDD3PS_Q$		V_{DDQ}	0.25	mA
IDD3N	$IDD3N_1$		V_{DD1}	1.5	mA
	$IDD3N_2$		V_{DD2}	17	mA
	$IDD3N_Q$		V_{DDQ}	0.25	mA
IDD3NS	$IDD3NS_1$		V_{DD1}	1.5	mA
	$IDD3NS_2$		V_{DD2}	15	mA
	$IDD3NS_Q$		V_{DDQ}	0.25	mA
IDD4R	$IDD4R_1$		V_{DD1}	4.75	mA
	$IDD4R_2$		V_{DD2}	235	mA
	$IDD4R_Q$		V_{DDQ}	105	mA
IDD4W	$IDD4W_1$		V_{DD1}	1.5	mA
	$IDD4W_2$		V_{DD2}	210	mA
	$IDD4W_Q$		V_{DDQ}	0.25	mA
IDD5	$IDD5_1$		V_{DD1}	27	mA
	$IDD5_2$		V_{DD2}	110	mA
	$IDD5_Q$		V_{DDQ}	0.25	mA
IDD5AB	$IDD5AB_1$		V_{DD1}	3	mA
	$IDD5AB_2$		V_{DD2}	20	mA
	$IDD5AB_Q$		V_{DDQ}	0.25	mA
IDD5PB	$IDD5PB_1$		V_{DD1}	3	mA
	$IDD5PB_2$		V_{DD2}	20	mA
	$IDD5PB_Q$		V_{DDQ}	0.25	mA
IDD6	$IDD6_1$	25°C	V_{DD1}	0.3	mA
		95°C		2.8	mA
	$IDD6_2$	25°C	V_{DD2}	0.7	mA
		95°C		12	mA
	$IDD6_Q$	25°C	V_{DDQ}	0.15	mA
		95°C		0.2	mA

Note:
1. These specification values are measured on single chip condition.

AC & DC Output Measurement Level

Single Ended AC and DC Output Level

Symbol	Parameter	Value			Unit	Note
		Under LPDDR4x-TBD Unterm	TBD to 3200 V_{SSQ} term	3200 to 4266 V_{SSQ} term		
$V_{OH(DC)}$	AC, DC Output High Measurement Level	V_{DDQ}	$V_{DDQ}/2$	$V_{DDQ}/2$	V	1
$V_{OL(DC)}$	AC, DC Output Low Measurement Level	V_{SSQ}	V_{SSQ}	V_{SSQ}	V	

Note:

1. 60ohm ODT value is assumed.

Pull Up/Pull Down Driver Characteristic and Calibration

Pull-down Driver Characteristic, with ZQ Calibration

RONPD,NOM	Resistor	Min	Nom	Max	Unit
40ohm	RON40PD	0.90	1.00	1.10	RZQ/6
48ohm	RON48PD	0.90	1.00	1.10	RZQ/5
60ohm	RON60PD	0.90	1.00	1.10	RZQ/4
80ohm	RON80PD	0.90	1.00	1.10	RZQ/3
120ohm	RON120PD	0.90	1.00	1.10	RZQ/2
240ohm	RON240PD	0.90	1.00	1.10	RZQ/1

Note:
1. All values are after ZQ Calibration. Without ZQ Calibration R_{ONPD} values are ±30%.

Pull-up Driver Characteristic, with ZQ Calibration

$V_{OHPU,nom}$	$V_{OH,nom}$ (mV)	Min	Nom	Max	Unit
V_{DDQ} x 0.5	300	0.90	1.00	1.10	$V_{OH,nom}$
V_{DDQ} x 0.6	360	0.90	1.00	1.10	$V_{OH,nom}$

Note:
1. All values are after ZQ Calibration. Without ZQ Calibration $V_{OH(nom)}$ values are ±30%.
2. $V_{OH,nom}$ values are based on a nominal V_{DDQ} = 0.6V.

Valid Calibration Point

$V_{OHPU,nom}$	ODT Value					
	240	120	80	60	48	40
V_{DDQ} x 0.5	VALID	VALID	VALID	VALID	VALID	VALID
V_{DDQ} x 0.6	DNU	VALID	DNU	VALID	DNU	DNU

Note:
1. Once the output is calibrated for a given $V_{OH(nom)}$ calibration point, the ODT value may be changed without recalibration.
2. If the $V_{OH(nom)}$ calibration point is changed, then re-calibration is required.
3. DNU = Do Not Use.

Pull-down Characteristic, without ZQ Calibration

RONPD,NOM	Resistor	V_{OUT}	Min	Nom	Max	Unit	Note
40ohm	RON40PD	0.5 x V_{OH}	0.70	1.00	1.10	RZQ/6	1
48ohm	RON48PD	0.5 x V_{OH}	0.70	1.00	1.30	RZQ/5	1

Note:
1. Across entire operating temperature range, without calibration.

Pull-up Characteristic, without ZQ Calibration (Die to Die Variation)

$V_{OHPU,nom}$	$V_{OH,nom}$ (mV)	Min	Nom	Max	Unit	Note
V_{DDQ} x 0.5	300	0.70	1.00	1.30	$V_{OH,nom}$	1
V_{DDQ} x 0.6	360	0.70	1.00	1.30	$V_{OH,nom}$	1

Note:
1. ODT value of Memory Controller should be informed with MRW before V_{OH} calibration.

V_{OUT} Level of un-terminated condition

Parameter	Symbol	Min	Max	Unit	Note
Output High Voltage Level when ODT of memory controller is turned off	V_{OH_unterm}	V_{DDQ} – 0.55	V_{DDQ} - 0.15	V	

Electrical Characteristic and AC Timing

Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR4x device.

Definition of tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK\ (avg) = \left(\sum_{j=1}^{N} tCK_j\right) \Big/ N$$,where N=200

Unit 'tCK(avg)' represents the actual clock average tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

tCK(avg) may change by up to ±1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

Definition of tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.
tCK(abs) is not subject to production test.

Definition of tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j\right) \Big/ [N \times tCK(avg)]$$ where N=200

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j\right) \Big/ [N \times tCK(avg)]$$ where N=200

Definition for tCH(abs) and tCL(abs)

tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
Both tCH(abs) and tCL(abs) are not subject to production test.

Definition for tJIT(per)

tJIT(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).
tJIT(per) = Min/max of {tCKi - tCK(avg) where i = 1 to 200}.
tJIT(per),act is the actual clock jitter for a given system.
tJIT(per),allowed is the specified allowed clock period jitter.
tJIT(per) is not subject to production test.

Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.
tJIT(cc) = Max of |{tCK(i +1)- tCK(i)}|.
tJIT(cc) defines the cycle to cycle jitter.
tJIT(cc) is not subject to production test.

Definition for tERR(nper)

tERR(nper) is defined as the cumulative error across n multiple consecutive cycles from tCK(avg).
tERR(nper),act is the actual clock jitter over n cycles for a given system.
tERR(nper),allowed is the specified allowed clock period jitter over n cycles.
tERR(nper) is not subject to production test.

$$tERR(nper) = \left(\sum_{j=1}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

tERR(nper),min can be calculated by the formula shown below:

$$tERR(nper), min = [(1 + 0.68\, LN(n)] \times tJIT(per), min$$

tERR(nper),max can be calculated by the formula shown below

$$tERR(nper), max = [(1 + 0.68\, LN(n)] \times tJIT(per), max$$

Using these equations, tERR(nper) tables can be generated for each tJIT(per),act value.

Definition for Duty Cycle jitter tJIT(duty)

tJIT(duty) is defined with absolute and average specification of tCH / tCL.

$$tJIT(duty), min = MIN[(tCH(abs), min - tCH(avg), min), (tCL(abs), min - tCL(avg), min)] \times tCK(avg)$$

$$tJIT(duty), max = MAX[(tCH(abs), max - tCH(avg), max), (tCL(abs), max - tCL(avg), max)] \times tCK(avg)$$

Definition for tCK(abs), tCH(abs) and tCL(abs)

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

Parameter	Symbol	Min	Unit
Absolute Clock Period	tCK(abs)	tCK(avg),min + tJIT(per),min	ps
Absolute Clock HIGH Pulse Width	tCH(abs)	tCH(avg),min + tJIT(duty),min / tCK(avg),min	tCK(avg)
Absolute Clock LOW Pulse Width	tCL(abs)	tCL(avg),min + tJIT(duty),min / tCK(avg),min	tCK(avg)

Note:
1. tCK(avg),min is expressed is ps for this table.
2. tJIT(duty),min is a negative value.

Period Clock Jitter

LPDDR4x devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter (tJIT(per)) in excess of the values found in Table of Valid Calibration Point. LPDDR4x AC Timing Table and how to determine cycle time de-rating and clock cycle de-rating.

Clock Period Jitter Effect on core timing parameter

(tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR4x device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}.

When the device is operated with clock jitter outside specification limits, the number of clocks or tCK(avg) may need to be increased based on the values for each core timing parameter.

Cycle Time De-rating for core timing parameter

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the amount of cycle time de-rating (in ns) required if the equation results in a positive value for a core timing parameter.

$$Cycle\ Timg\ Derating = MAX\left\{\left[\frac{tPARAM + tERR(tnPARAM), act - tERR(tNPARAM), allowed}{tnPARAM}\right], 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

Clock Cycle De-rating for core timing parameter

For a given number of clocks (tnPARAM) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter (tJIT(per)).

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter.

$$Clock\ Cycle\ Derating = RU\left[\frac{tPARAM + tERR(tnPARAM), act - tERR(tNPARAM), allowed}{tCK(avg)}\right] - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

Clock Jitter Effect on Command/Address timing parameter

Command/address timing parameters (tIS, tIH, tISb, tIHb) are measured from a command/address signal (CS or CA[5:0]) transition edge to its respective clock signal (CK_t/CK_c) crossing. The specification values are not affected by the tJIT(per) applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

Clock Jitter Effect on Read timing parameter

tRPRE

When the device is operated with input clock jitter, tRPRE needs to be de-rated by the actual period jitter (tJIT(per),act_{max}) of the input clock in excess of the allowed period jitter (tJIT(per),$allowed_{max}$). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left[\frac{tJIT(per), act_{max} - tJIT(per), allowed_{max}}{tCK(avg)}\right]$$

For example,
if the measured jitter into a LPDDR4x device has tCK(avg) = 625ps, tJIT(per),act_{min} = -xx, and tJIT(per),act_{max} = +xx ps, then:
$tRPRE_{min}$,derated = 0.9 - (tJIT(per),act_{max} - tJIT(per),$allowed_{max}$)/tCK(avg) = 0.9 - (xx - xx)/xx = yy tCK(avg).

tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. tJIT(per).

tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min.
These parameters determine the absolute Data-Valid window(DVW) at the LPDDR4x device pin.
Absolute min DVW @LPDDR4x device pin = min { (tQSH(abs)min – tDQSQmax), (tQSL(abs)min – tDQSQmax) }
This minimum DVW shall be met at the target frequency regardless of clock jitter.

tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.
tRPST(abs)min = tCL(abs)min – 0.05 = tQSL(abs)min

Clock jitter effects on Write timing parameter

tDS, tDH

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition edge to its respective data strobe signal (DQSn_t, DQSn_c : n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the data strobe signal crossing that latches the data. Regardless of clock jitter values, these values shall be met.

tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx_t, DQSx_c) crossing to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per)), as the setup and hold of the data strobes are relative to the corresponding clock signal crossing. Regardless of clock jitter values, these values shall be met.

tDQSS

This parameter is measured from a data strobe signal (DQSx_t, DQSx_c) crossing to the subsequent clock signal (CK_t/CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter tJIT(per),act of the input clock in excess of the allowed period jitter tJIT(per),allowed.

$$tDQSS(min, derated) = 0.75 - \left[\frac{tJIT(per), act_{min} - tJIT(per), allowed_{min}}{tCK(avg)}\right]$$

$$tDQSS(max, derated) = 1.25 - \left[\frac{tJIT(per), act_{min} - tJIT(per), allowed_{min}}{tCK(avg)}\right]$$

For example,
if the measured jitter into an LPDDR4x device has tCK(avg) = 625ps, tJIT(per),act_{min} = -xxps, and tJIT(per),act_{max} = +xx ps, then:
tDQSS,(min,derated) = 0.75 - (-xx + yy)/625 = xxxx tCK(avg)
tDQSS,(max,derated) = 1.25 - (xx . yy)/625 = xxxx tCK(avg)

LPDDR4x Refresh Requirement

Parameter		Symbol	4Gb	Unit
Density per Channel		-	4	Gb
Number of Banks per Channel		-	8	-
Refresh Window, T_{CASE} ≤ 85°C		tREFW	32	ms
Refresh Window, 1/2-Rate Refresh		tREFW	16	ms
Refresh Window, 1/4-Rate Refresh		tREFW	8	ms
Required number of Refresh Command in a tREFW window (min)		R	8,192	-
Average Refresh Internal	REFab	tREFI[3]	3,904	us
	REFpb	tREFIpb	488	ns
Refresh Cycle Time (All Banks)		tRFCab	180	ns
Refresh Cycle Time (Per Bank)		tRFCpb	90	ns
Per-bank Refresh to Per-bank Refresh different Bank Time		tpbR2pbR	90	ns

Note:

1. Refresh for each channel is independent of the other channel on the die, or other channels in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.
2. Self Refresh abort feature is available for higher density devices starting with 12Gb dual channel device and 6Gb single channel device and tXSR_abort(min) is defined as tRFCpb + 17.5ns.
3. tREFI values for all bank refresh is T_{CASE} = -40 to 85°C, T_{CASE} means Operating Case Temperature.

AC Timing

Parameter	Symbol	Min/Max	LPDDR4x 4266	Unit
Maximum Clock Frequency	-	-	2133	MHz
Clock Timing				
Average Clock Period	tCK(avg)	Min	0.468	ns
		Max	100	ns
Average HIGH Pulse Width	tCH(avg)	Min	0.45	tCK(avg)
		Max	0.55	tCK(avg)
Average LOW Pulse Width	tCL(avg)	Min	0.45	tCK(avg)
		Max	0.55	tCK(avg)
Absolute Clock Period	tCK(abs)	Min	tCK(avg)min + tJIT(per)min	ns
Absolute HIGH Clock Pulse Width	tCH(abs)	Min	0.43	tCK(avg)
		Max	0.57	tCK(avg)
Absolute LOW Clock Pulse Width	tCL(abs)	Min	0.43	tCK(avg)
		Max	0.57	tCK(avg)
Clock Period Jitter	tJIT(per)	Min	-30	ps
		Max	30	ps
Maximum Clock Jitter between two consecutive cycles	tJIT(cc)	Max	60	ps
Duty Cycle Jitter (with supported Jitter)	tJIT(duty), allowed	Min	Min((tCH(abs),min – tCH(avg),min,(tCL(abs),min – tCL(avg),min)) x tCK(avg)	ps
		Max	Max((tCH(abs),max – tCH(avg),max,(tCL(abs),max – tCL(avg),max)) x tCK(avg)	ps
Core Parameter [17]				
Read Latency (no DBI)	RL	Min	36	tCK(avg)
Write Latency (set A)	WL	Min	18	tCK(avg)
Activate-to-Activate Command Period (same Bank)	tRC	Min	tRAS + tRPab (with all-bank precharge) tRAS + tRPpb (with per-bank precharge)	ns
Minimum Self-Refresh Time (Entry to Exit)	tSR	Min	Max(15ns, 3tCK)	ns
Self Refresh exit to next valid Command Delay	tXSR	Min	Max (tRFCab + 7.5ns, 2tCK)	ns
Exit Power Down to next valid Command Delay	tXP	Min	Max(7.5ns, 5tCK)	ns
CAS-to-CAS Delay	tCCD	Min	BL/2	tCK(avg)
CAS to CAS Delay Masked Write	tCCDMW[31]	Min	4 × tCCD	tCK(avg)
Internal READ to PRECHARGE command delay	tRTP	Min	Max(7.5ns, 8tCK)	ns
RAS-to-CAS delay	tRCD	Min	Max(18ns, 4tCK)	ns
Row Precharge Time (single bank)	tRPpb	Min	Max(18ns, 4tCK)	ns
Row Precharge Time (all banks)	tRPab	Min	Max(21ns, 4tCK)	ns
Row Active Time	tRAS	Min	Max(42ns, 3tCK)	ns
		Max	Min(9 x tREFI x Refresh Rate[19], 70.2)	us
Write Recovery Time	tWR	MIN	Max(18ns,6tCK)	ns
Write-to-Read Delay	tWTR	MIN	Max(10ns,8tCK)	ns
Active Bank-A to Active Bank-B	tRRD	MIN	Max(10ns,4tCK)	ns
Precharge-to-Precharge Delay	tPPD	MIN	4	tCK
Four-Bank Activate Window	tFAW	MIN	40	ns

Parameter	Symbol	Min/Max	LPDDR4x 4266	Unit
CKE minimum Pulse Width during Self Refresh (Low Pulse Width during Self Refresh)	tCKELPD	MIN	Max(7.5ns, 3tCK)	ns
Read Parameter[4]				
Read Preamble	tRPRE[5,8]	Min	2.0	tCK(avg)
0.5 tCK Read Postamble	tRPST[5,9]	Min	0.5	tCK(avg)
1.5 tCK Read Postamble	tRPST	Min	1.5	tCK(avg)
DQ Low-Impedance Time from CK_t, CK_c	tLZ(DQ)[5]	Min	(RL × tCK) + tDQSCK(Min) - 200ps	ps
DQ High Impedance Time from CK_t, CK_c	tHZ(DQ)[5]	Max	(RL × tCK) + tDQSCK(Max) + tDQSQ(Max) + (BL/2 × tCK) - 100ps	ps
DQS_c Low-Impedance Time from CK_t, CK_c	tLZ(DQS)[5]	Min	(RL × tCK) + tDQSCK(Min) - (tPRE(Max) × tCK) - 200ps	ps
DQS_c High Impedance Time from CK_t, CK_c	tHZ(DQS)[5]	Max	(RL × tCK) + tDQSCK(Max)+ (BL/2 × tCK) - (RPST(Max) × tCK) - 100ps	ps
DQS-DQ Skew	tDQSQ	Max	0.18	UI
tDQSCK Parameter				
DQS Output Access Time from CK_t/CK_c	tDQSCK[14]	Min	1500	ps
		Max	3500	ps
DQS Output Access Time from CK_t/CK_c Temperature Variation	tDQSCK_temp[15]	Max	4	ps/°C
DQS Output Access Time from CK_t/CK_c Voltage Variation	tDQSCK_volt[16]	Max	7	ps/mV
CK to DQS Rank-to-Rank Variation	tDQSCK_rank2rank[22,23]	Max	1.0	ns
Self Refresh Parameter				
Delay from SRE command to CKE Input Low	tESCKE[24]	Min	Max(1.75ns, 3nCK)	ns
Minimum Self Refresh Time	tSR[24]	Min	Max(15ns, 3tCK)	ns
Exit Self Refresh to Valid commands	tXSR[24,25]	Min	Max(tRFCab + 7.5ns, 2tCK)	ns
Write Parameter[4]				
Write command to 1st DQS Latching	tDQSS	Min	0.75	tCK(avg)
		Max	1.25	
DQS Input High-Level Width	tDQSH	Min	0.4	tCK(avg)
DQS Input Low-Level Width	tDQSL	Min	0.4	tCK(avg)
DQS Falling edge to CK Setup Time	tDSS	Min	0.2	tCK(avg)
DQS Falling edge Hold Time from CK	tDSH	Min	0.2	tCK(avg)
Write Preamble	tWPRE	Min	2.0	tCK(avg)
0.5 tCK Write Postamble	tWPST[21]	Min	0.5	tCK(avg)
1.5 tCK Write Postamble	tWPST[21]	Min	1.5	tCK(avg)
ZQ Calibration Parameter				
ZQ Calibration	tZQCAL	Min	1	Us
ZQ Calibration Values Latch Time	tZQLAT	Min	Max(30ns, 8tCK)	ns
ZQ Calibration RESET Time	tZQRESET	Min	Max(50ns, 3tCK)	ns
Power Down Parameter				
CKE minimum Pulse Width (HIGH and LOW Pulse Width)	tCKE	Min	Max(7.5ns, 4tCK)	ns
Delay from Valid command to CKE Input Low	tCMDCKE[26]	Min	Max(1.75ns, 3tCK)	ns
Valid Clock Requirement after CKE Input Low	tCKELCK[26]	Min	Max(5ns, 5tCK)	-
Valid CS Requirement before CKE Input Low	tCSCKE	Min	1.75	ns

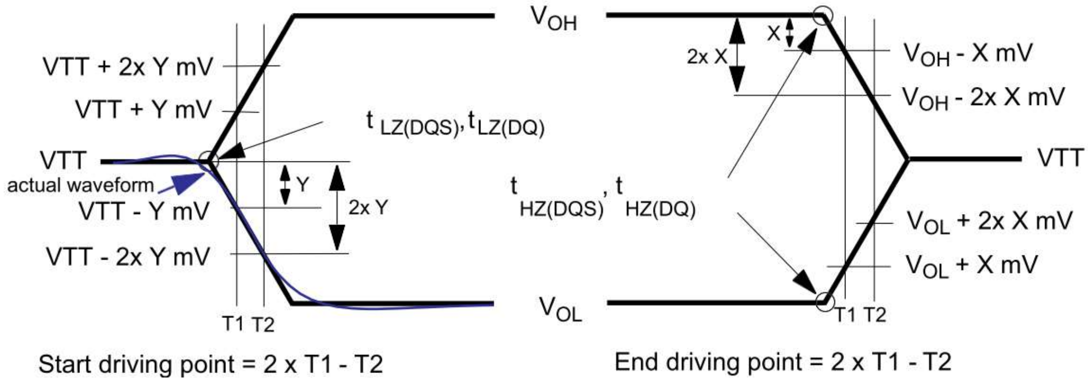
Parameter	Symbol	Min/Max	LPDDR4x 4266	Unit
Valid CS Requirement after CKE Input Low	tCKELCS	Min	Max(5ns, 5tCK)	ns
Valid Clock Requirement before CKE Input High	tCKCKEH[26]	Min	Max(1.75ns, 3tCK)	ns
Exit Power-Down to next valid command Delay	tXP[26]	Min	Max(7.5ns, 5tCK)	ns
Valid CS Requirement before CKE Input High	tCSCKEH	Min	1.75	ns
Valid CS Requirement after CKE Input High	tCKEHCS	Min	Max(7.5ns,5tCK)	ns
Valid Clock and CS Requirement after CKE Input Low after MRW Command	tMR_{WCKEL}[26]	Min	Max(14ns,10tCK)	ns
Valid Clock and CS Requirement after CKE Input Low after ZQ Calibration Start Command	tZQCKE[26]	Min	Max(1.75ns,3tCK)	ns
Command Address Input Parameter[4]				
Rx Mask Voltage, P-P	V_{cIVW}	Max	145	mV
Rx Timing Window	TcIVW	Max	0.3	UI*
CA AC Input Pulse Amplitude Pk-Pk	V_{IHL_AC}	Min	180	mV
CA Input Pulse Width	TcIPW	Min	0.6	UI*
Input Slew Rate over VcIVW	SRIN_cIVW	Min	1	V/ns
		Max	7	V/ns
Mode Register Read/Write AC Timing				
Additional Time after tXP has expired until MRR command	tMRRI	Min	tRCD + 3nCK	-
Mode Register Read command period	tMRR	Min	8	nCK
Mode Register Write command period	tMRW	Min	Max(10ns, 10nCK)	-
Mode Register Set command delay	tMRD	Min	Max(14ns, 10tCK)	-
Boot Parameter (10MHz – 55MHz)[11,12,13]				
Clock Cycle Time	tCKb	Max	100	ns
		Min	18	ns
Address & Control Input Setup Time	tISb	Min	1150	ps
Address & Control Input Hold Time	tIHb	Min	1150	ps
DQS Output Data Access Time from CK_t/CK_c	tDQSCKb	Min	2.0	ns
		Max	10.0	ns
Data Strobe Edge to Output Data Edge	tDQSQb	Max	1.2	ns
Command Bus Training AC Parameter				
Valid Clock Requirement after CKE Input low	tCKELCK	Min	Max(5ns, 5nCK)	tCK
Data Setup for VREF Training Mode	tDStrain	Min	2	ns
Data Hold for VREF Training Mode	tDHtrain	Min	2	ns
Asynchronous Data Read	tADR	Max	20	ns
CA Bus Training command to CA Bus Training command delay	tCACD[29]	Min	RU(tADR/tCK)	tCK
Valid Strobe Requirement before CKE Low	tDQSCKE[30]	Min	10	ns
First CA Bus Training Command Following CKE LOW	tCAENT	Min	250	ns
VREF Step Time-Multiple Step	tVREFCA _LONG	Max	250	ns
VREF Step Time-One Step	tVREFCA __SHORT	Max	80	ns
Valid Clock Requirement before CS High	tCKPRECS	Min	2tCK + tXP (tXP = Max(7.5ns, 5nCK))	-
Valid Strobe Requirement before CKE Low	tDQSCKE[30]	Min	10	ns
First CA Bus Training Command following CKE Low	tCAENT	Min	250	ns

Parameter	Symbol	Min/Max	LPDDR4x 4266	Unit
VREF Step Time-Multiple Step	tVREFCA _LONG	Max	250	ns
VREF Step Time-One Step	tVREFCA _SHORT	Max	80	ns
Valid Clock Requirement before CS High	tCKPRECS	Min	2tCK + tXP (tXP = max(7.5ns, 5nCK))	-
Valid Clock Requirement after CS High	tCKPSTCS	Min	max(7.5ns, 5nCK)	-
Minimum delay from CS to DQS Toggle in command bus training	tCS_VREF	Min	2	tCK
Minimum delay from CKE High to Strobe High Impedance	tCKEHDQS	-	10	ns
Valid Clock Requirement before CKE Input High	tCKCKEH	Min	Max(1.75ns, 3tCK)	
CA Bus Training CKE High to DQ Tri-state	tMRZ	Min	1.5	ns
ODT turn-on Latency from CKE	tCKELODTon	MIN	20	ns
ODT turn-off Latency from CKE	tCKELODToff	MIN	20	ns
Exit Command Bus Training Mode to next Valid command delay[32]	tXCBT_Short	Min	Max(5nCK, 200ns)	-
	tXCBT_Middle	Min	Max(5nCK, 200ns)	-
	tXCBT_Long	Min	Max(5nCK, 250ns)	-
Write Leveling Parameter				
DQS_t/DQS_c Delay after Write Leveling mode is programmed	tWLDQSEN	Min	20	tCK
Write Preamble for Write Leveling	tWLWPRE	Min	20	tCK
First DQS_t/DQS_c edge after Write Leveling mode is programmed	tWLMRD	Min	40	tCK
Write Leveling Output Delay	tWLO	Max	20	ns
Mode Register Set Command Delay	tMRD	Min	Max(14ns, 10tCK)	ns
Valid Clock Requirement before DQS Toggle	tCKPRDQS	Min	Max(7.5ns, 4tCK)	-
Valid Clock Requirement after DQS Toggle	tCKPSTDQS	Min	Max(7.5ns, 4tCK)	-
Write Leveling Hold Time	tWLH[27]	Min	50	ps
Write Leveling Setup Time	tWLS[27]	Min	50	ps
Write Leveling Input Valid Window	tWLIVW[28]	Min	90	ps
Temperature De-Rating AC Time[20]				
DQS Output Access Time from CK_t/CK_c (Derated)	tDQSCK	Max	3600	ps
RAS-to-CAS Delay (Derated)	tRCD	Min	tRCD + 1.875	ns
Activate-to- Activate Command Period (Derated)	tRC	Min	tRC + 3.75	ns
Row Active Time (Derated)	tRAS	Min	tRAS + 1.875	ns
Row Precharge Time (Derated)	tRP	Min	tRP + 1.875	ns
Active Bank A to Active Bank B (Derated)	tRRD	Min	tRRD + 1.875	ns

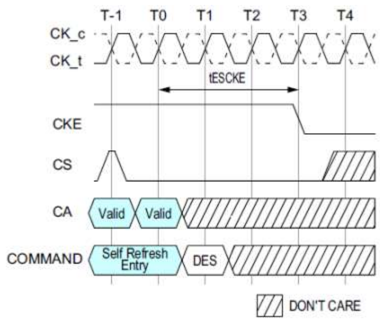
Note:

1. Frequency values are for reference only. Clock cycle time (tCK) is used to determine device capabilities.
2. All AC timings assume an input slew rate of TBDV/ns.
3. Measured with 4 V/ns differential CK_t/CK_c slew rate and nominal V_{IX}.
4. READ, WRITE, and Input setup and hold values are referenced to V_{REF}.
5. For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (V_{TT}). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Operating and Timing [Burst Read:RL=12, BL=8, tDQSCK<tCK] shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

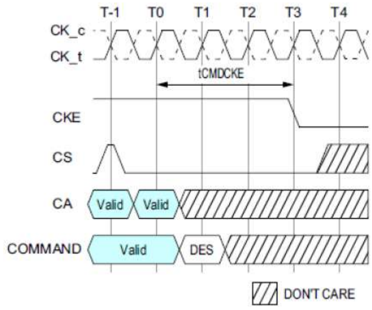
6. Output Transition Timing



7. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS_t-DQS_c.
8. Measured from the point when DQS_t/DQS_c begins driving the signal to the point when DQS_t/DQS_c begins driving the first rising strobe edge. See Pre and Post-amble section in Operating & Timing spec
9. Measured from the last falling strobe edge of DQS_t/DQS_c to the point when DQS_t/DQS_c finishes driving the signal.
10. Input set-up/hold time for signal (CA[9:0], CS).
11. To ensure device operation before the device is configured, a number of AC boot-timing parameters are defined in this table. Boot parameter symbols have the letter b appended (for example, tCK during boot is tCKb).
12. The LPDDR4x device will set some default values upon receiving a RESET (MRW) command as specified in "Definition".
13. The output skew parameters are measured with default output impedance settings using the reference load.
14. Includes DRAM process, voltage, and temperature variation. It includes the AC noise impact for frequencies > 20 MHz and max voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC Operating conditions.
15. tDQSCK_temp max delay variation as a function of Temperature.
16. tDQSCK_volt max delay variation as a function of DC voltage variation for V_{DDQ} and V_{DD2}. tDQSCK_volt should be used to calculate timing variation due to V_{DDQ} and V_{DD2} noise < 20 MHz. Host controller does not need to account for any variation due to V_{DDQ} and V_{DD2} noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the Max[abs{tDQSCKmin@V1-tDQSCKmax@V2}, abs{tDQSCKmax@V1-tDQSCKmin@V2}]/ abs{V1-V2}.
17. Precharge to precharge timing restriction does not apply to Auto-Precharge commands.
18. tXSR/tXP/tZQLAT are defined as "to the first rising clock edge next valid command".
19. Refresh Rate is specified by MR4, OP[2:0].
20. Timing derating applies for operation at 85°C to 105°C.
21. The length of Write Postamble depends on MR3 OP1 setting.
22. The same voltage and temperature are applied to tDQS2CK_rank2rank.
23. tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
24. Delay time has to satisfy both analog time(ns) and clock count(tCK).
It means that tESCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired. The case which 3tCK is applied to is shown below.

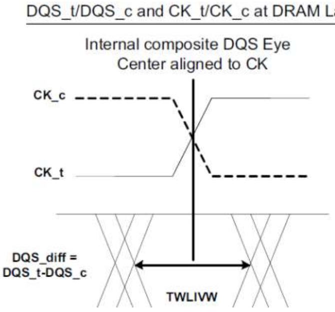


25. MRR-1, CAS-2, DES, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting are only allowed during this period.
26. Delay time has to satisfy both analog time(ns) and clock count(nCK).
For example, tCMDCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired. The case which 3nCK is applied to is shown below.



27. In addition to the traditional setup and hold time specifications above, there is value in a input valid window based specification for write-leveling training. As the training is based on each device, worst case process skews for setup and hold do not make sense to close timing between CK and DQS.

28. tWLIVW is defined in a similar manner to tdIVW_Total, except that here it is a DQS input valid window with respect to CK. This would need to account for all VT (voltage and temperature) drift terms between CK and DQS within the DRAM that affect the write-leveling input valid window.
The DQS input mask for timing with respect to CK is shown in Figure 25. The "total" mask (tWLIVW) defines the time the input signal must not encroach in order for the DQS input to be successfully captured by CK with a BER of lower than TBD. The mask is a receiver property and it is not the valid data-eye.

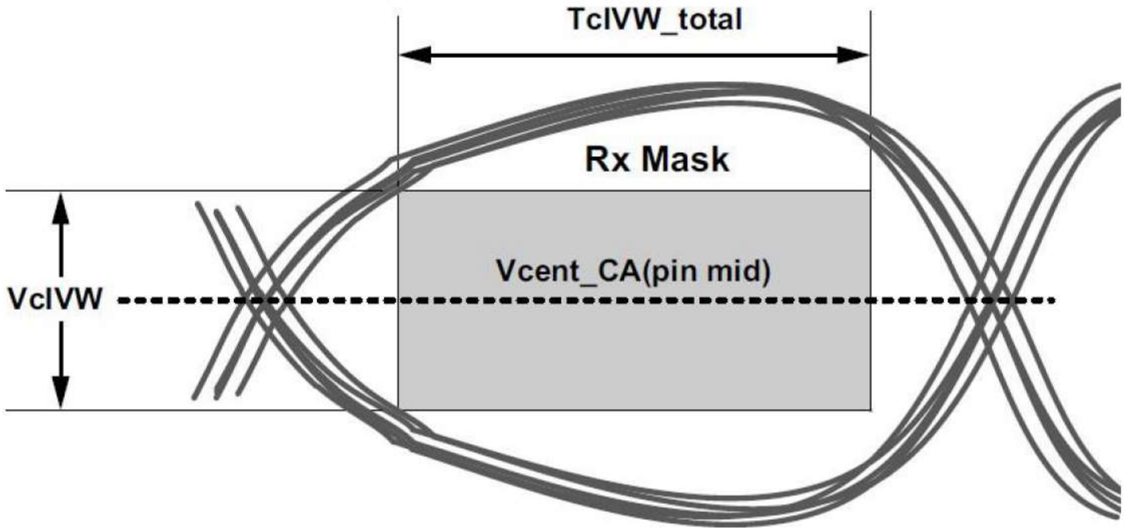


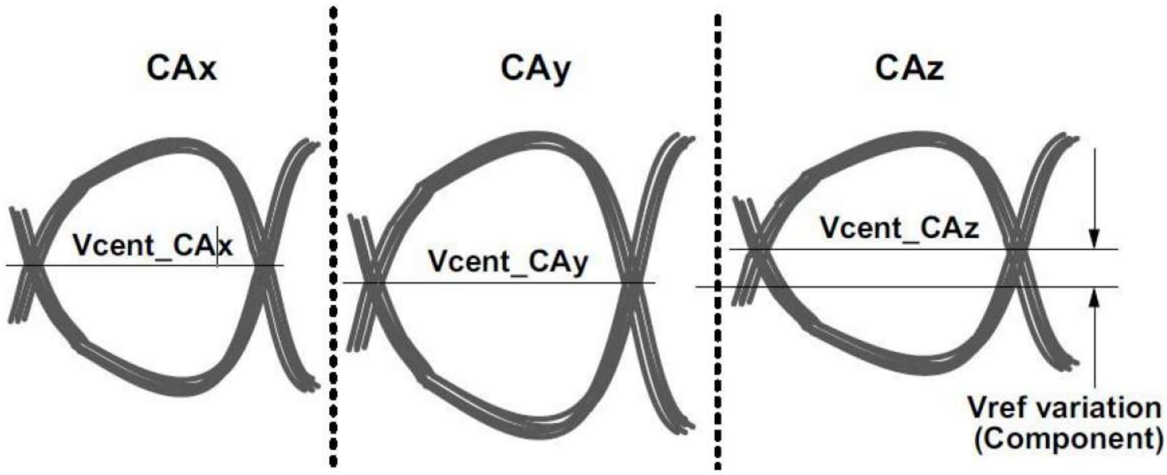
29. If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.
30. DQS_t has to retain a low level during tDQSCKE period, as well as DQS_c has to retain a high level.
31. See Masked Write Operation for detail.
32. Precharge to precharge timing restriction does not apply to Auto-Precharge commands.
33. Exit Command Bus Training Mode to next valid command delay Time depends on value of V_{REFCA} setting: MR12 OP[5:0] and V_{REFCA} Range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in tFC value mapping table. Additionally, exit Command Bus Training Mode to next valid command delay Time may affect V_{REFDQ} setting. Settling time of V_{REFDQ} level is same as V_{REFCA} level.

CA Rx Voltage and Timing

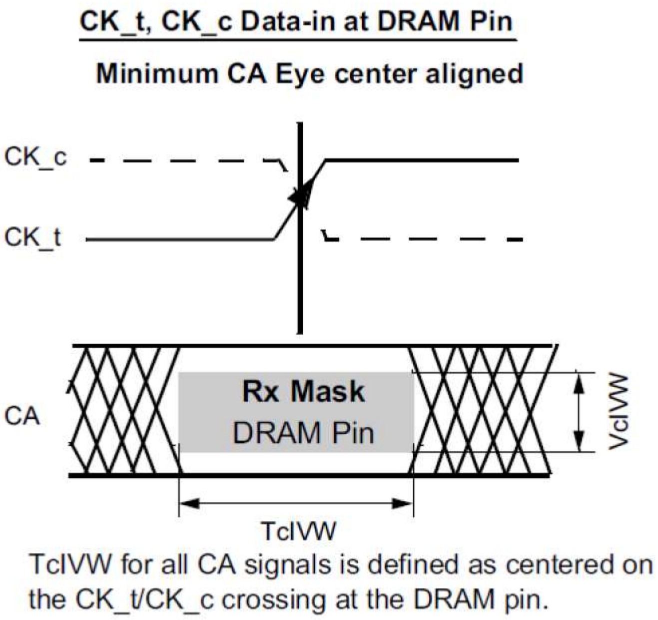
The command and address (CA) including CS input receiver compliance mask for voltage and timing is shown in the figure below. All CA, CS signals apply the same compliance mask and operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in the figure below is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

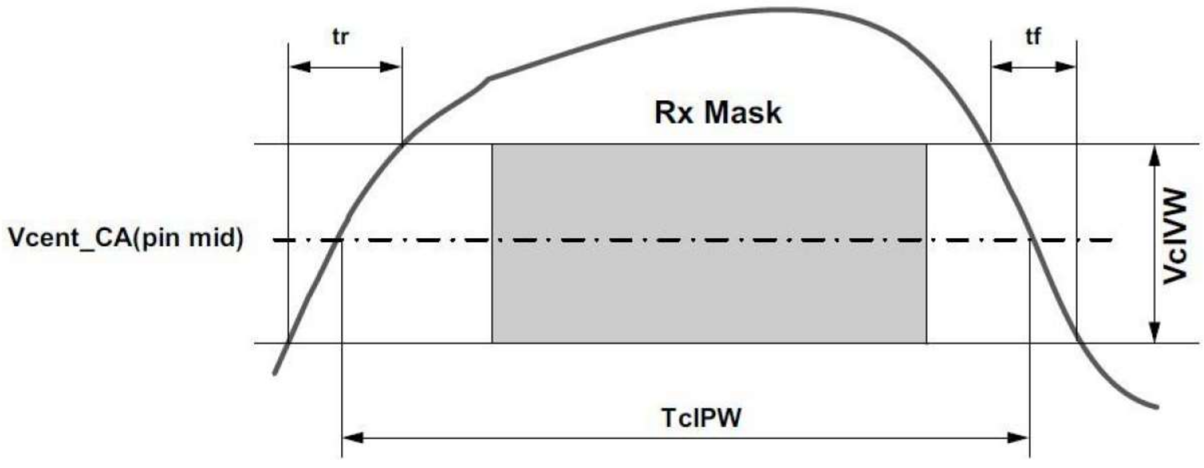




$V_{cent\_CA(pin\ avg)}$ is defined as the midpoint between the largest V_{cent_CA} voltage level and the smallest V_{cent_CA} voltage level across all CA and CS pins for a given DRAM component. Each CA V_{cent} level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in above figure. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask. The component level V_{REF} will be set by the system to account for Ron and ODT settings.

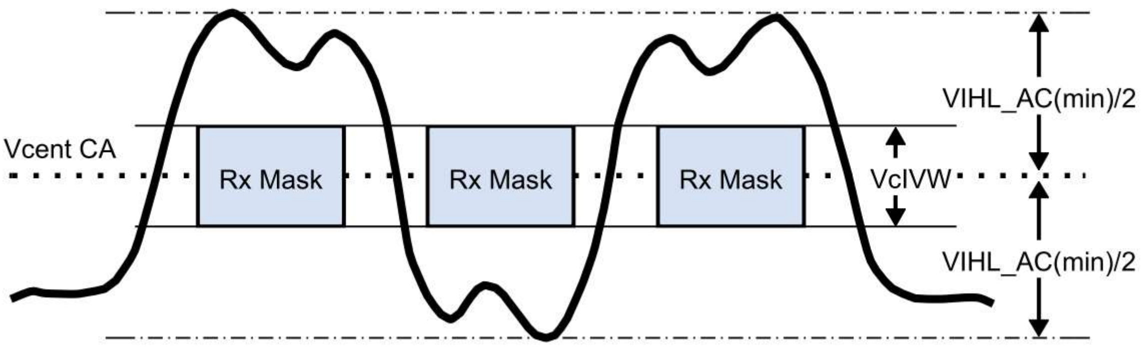


All of the timing terms in above figure. are measured from the CK_t/CK_c to the center(midpoint) of the TcIVW window taken at the $V_{cIVW\_total\ voltage}$ levels centered around $V_{cent\_CA(pin\ mid)}$.



Note:

1. SRIN_cIVW=V_{cIVW_Total} / (tr or tf), signal must be monotonic within tr and tf range.



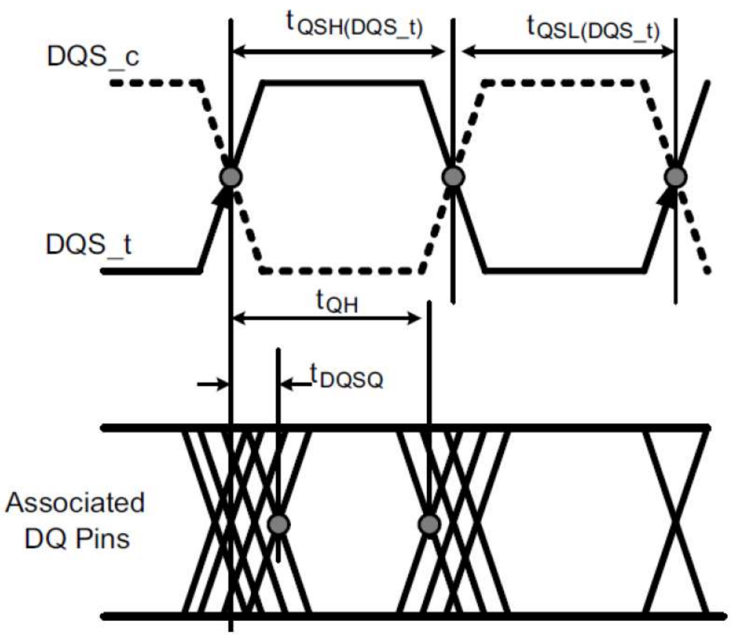
Symbol	Parameter	4266		Unit	Note
		Min	Max		
V_{clVW}	Rx Mask Voltage P-P	-	145	mV	1,2,3
TclVW	Rx Timing Window	-	0.3	UI*	1,2,3
V_{IHL_AC}	CA AC Input Pulse Amplitude Pk-Pk	180	-	mV	4,7
TclPW	CA Input Pulse Width	0.6	-	UI*	5
SRIN_clVW	Input Slew Rate over VclVW	1	7	V/ns	6

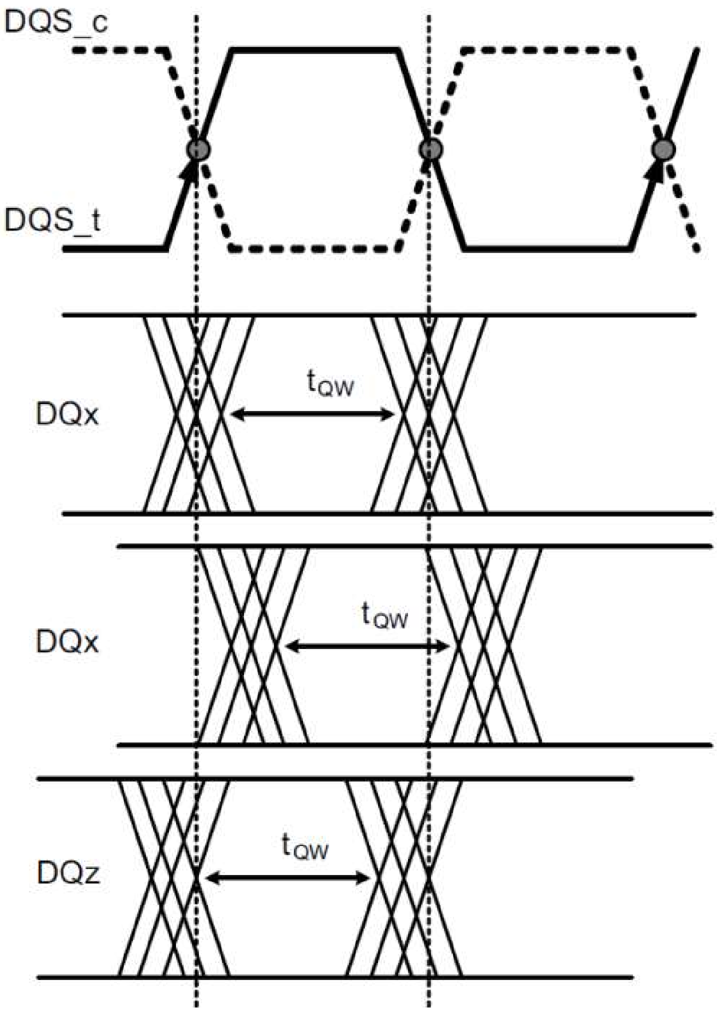
***UI = tCK(avg)min**

Note:

1. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2. Rx mask voltage $V_{clVW\ total(max)}$ must be centered around $V_{cent\_CA(pin\ mid)}$.
3. V_{cent_CA} must be within the adjustment range of the CA internal V_{REF}.
4. CA only input pulse signal amplitude into the receiver must meet or exceed V_{IHL_AC} at any point over the total UI. No timing requirement above level. V_{IHL_AC} is the peak to peak voltage centered around $V_{cent\_CA(pin\ mid)}$ such that V_{IHL_AC} /2 min must be met both above and below V_{cent_CA}.
5. CA only minimum input pulse width defined at the $V_{cent\_CA(pin\ mid)}$.
6. Input slew rate over V_{clVW} Mask centered at $V_{cent\_CA(pin\ mid)}$.
7. V_{IHL_AC} does not have to be met when no transitions are occurring.

DRAM Data Timing




DQS_c
DQS_t
DQx
tQW
DQx
tQW
DQz
tQW

Parameter	Symbol	4266		Unit	Note
		Min	Max		
Data Timing					
DQS_t, DQS_c to DQ Skew total, per group, per access (DBI disabled)	tDQSQ	-	0.18	UI	
DQ Output Hold Time total from DQS_t, DQS_c (DBI disabled)	tQH	Min(tQHS, tQSL)	-	UI	
DQ Ouput Window Time total, per pin (DBI disabled)	tQW_total	0.7	-	UI	3
DQ Output Window Time deterministic, per pin (DBI disabled)	tQW_dj	-	TBD	UI	2,3
DQS_t, DQS_c to DQ Skew total, per group, per access (DBI enabled)	tDQSQ_DBI	-	0.18	UI	
DQ Output Hold Time total from DQS_t, DQS_c (DBI enabled)	tQH_DBI	Min(tQSH_DBI, tQSL_DBI)	TBD	UI	
DQ Output Window Time total, per pin (DBI enabled)	tQW_total_DBI	0.7	-	UI	3
Data Strobe Timing					
DQS_t, DQS_c Differential Output Low Time (DBI disabled)	tQSH	tCL(abs) – 0.05	-	tCK(avg)	3,4
DQS_t, DQS_c Differential Output High Time (DBI disabled)	tQSL	tCH(abs) – 0.05	-	tCK(avg)	3,5
DQS_t, DQS_c Differential Output Low Time (DBI enabled)	tQSH_DBI	tCL(abs) – 0.045	-	tCK(avg)	4,6
DQS_t, DQS_c Differential Output High Time (DBI enabled)	tQSL_DBI	tCH(abs) – 0.045	-	tCK(avg)	5,6

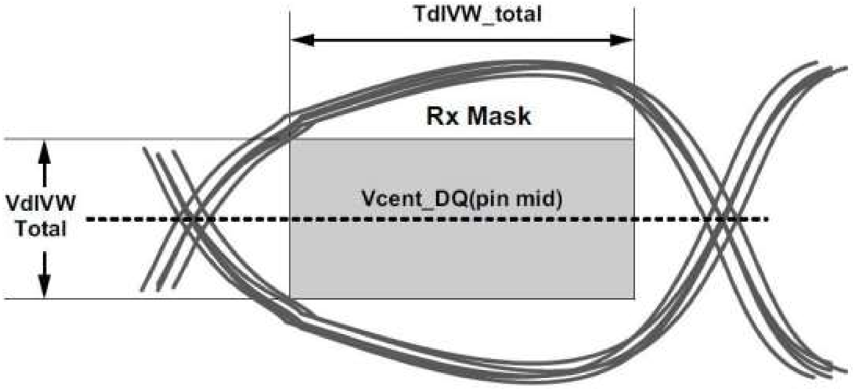
UI = tCK(avg)min

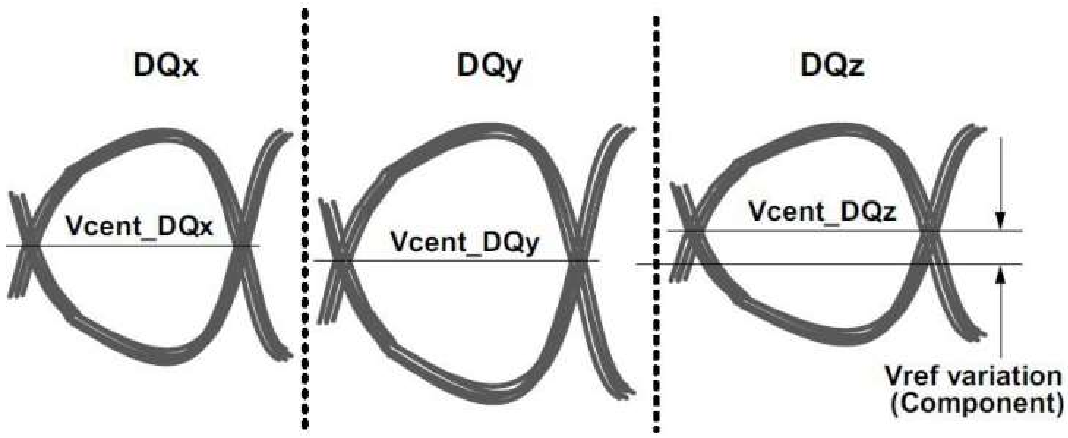
Note:

1. The deterministic component of the total timing. Measurement method tbd.
2. This parameter will be characterized and guaranteed by design.
3. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tCK(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.
4. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.
5. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.
6. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tCK(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.

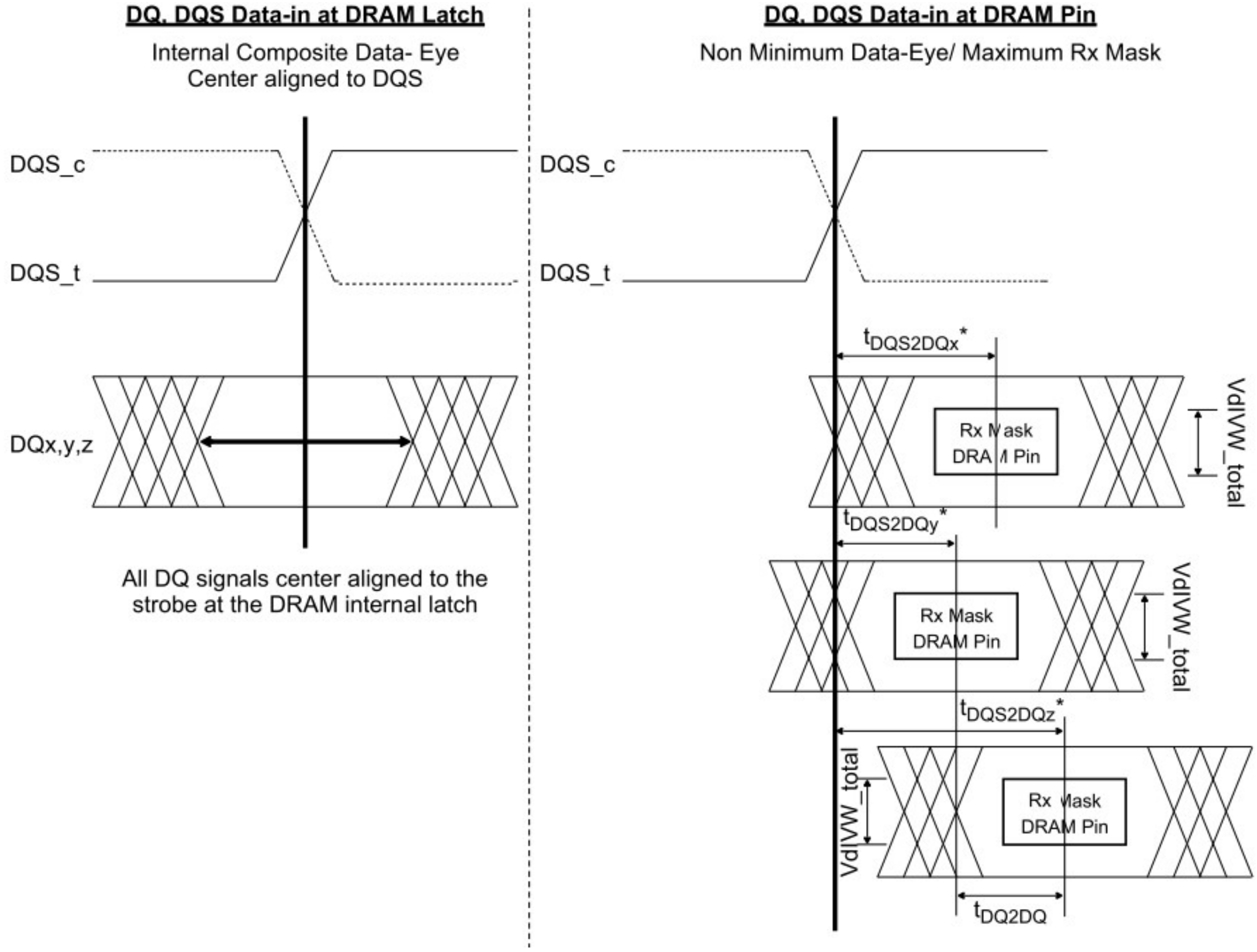
DQ Rx Voltage and Timing

The DQ input receiver mask for voltage and timing is shown Figure 33. is applied per pin. The “total” mask (V_{dIVW_total}, TdiVW_total) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal with a BER of lower than TBD. The mask is a receiver property and it is not the valid data-eye.

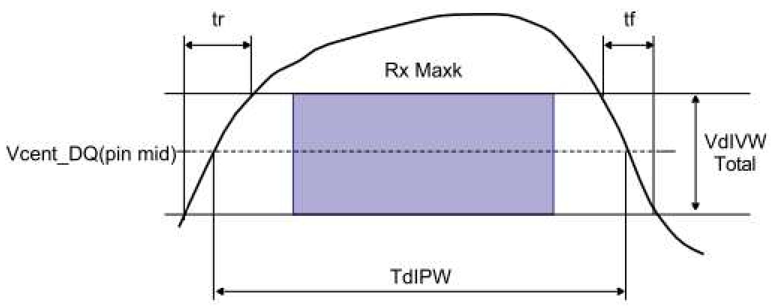




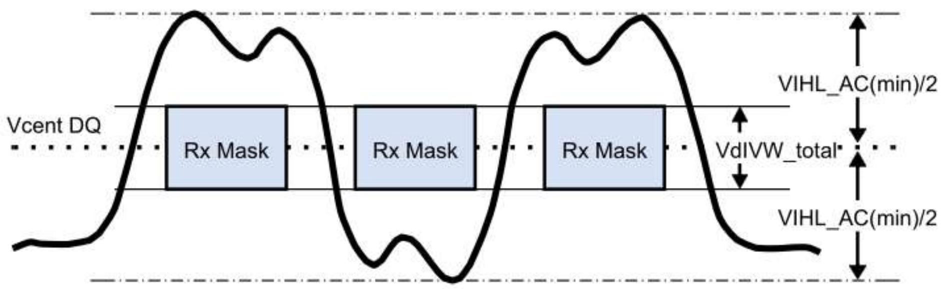
$V_{cent\_DQ(pin\ mid)}$ is defined as the midpoint between the largest V_{cent_DQ} voltage level and the smallest V_{cent_DQ} voltage level across all DQ pins for a given DRAM component. Each DQ V_{cent} is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in above figure. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level V_{REF} will be set by the system to account for Ron and ODT settings.



Note:
1. tDQS2DQ is measured at the center (midpoint) of the TdiVW window.
2. DQz represents the max tDQS2DQ in this example.
3. DQy represents the min tDQS2DQ in this example.



Note:
1. SRIN_dIVW = V_{dIVW_total} / (tr ot tf), signal must be monotonic within tr and tf range.



Parameter	Symbol	4266		Unit	Note
		Min	Max		
Rx Mask Voltage, P-P total	V_{dIVW_total}	-	120	mV	1,2,3,4
Rx Timing Window Total (at V_{dIVW} Voltage level)	TdIVW_total	-	0.25	UI*	1,2,4
Rx Timing Window 1 bit Toggle (at V_{dIVW} Voltage level)	TdIVW_1bit	-	TBD	UI*	1,2,4,12
DQ AC Input Pulse Amplitude, Pk-Pk	V_{IHL_AC}	170	-	mV	5,13
Input Pulse Width (at V_{cent_DQ})	TdIPW DQ	0.45	-	UI*	6
DQ to DQS offset	tDQS2DQ	200	800	ps	7
DQ to DQ offset	tDQ2DQ	-	30	ps	8
DQ to DQS offset Temperature variation	tDQS2DQ_temp	-	0.6	ps/°C	9
DQ to DQS offset Voltage variation	tDQS2DQ_volt	-	33	ps/50mV	10
Input Slew Rate over V_{dIVW_total}	SRIN_dIVW	1	7	V/ns	11
DQ to DQS offset Rank to Rank variation	tDQS2DQ_rank2rank	-	200	ps	14,15,16

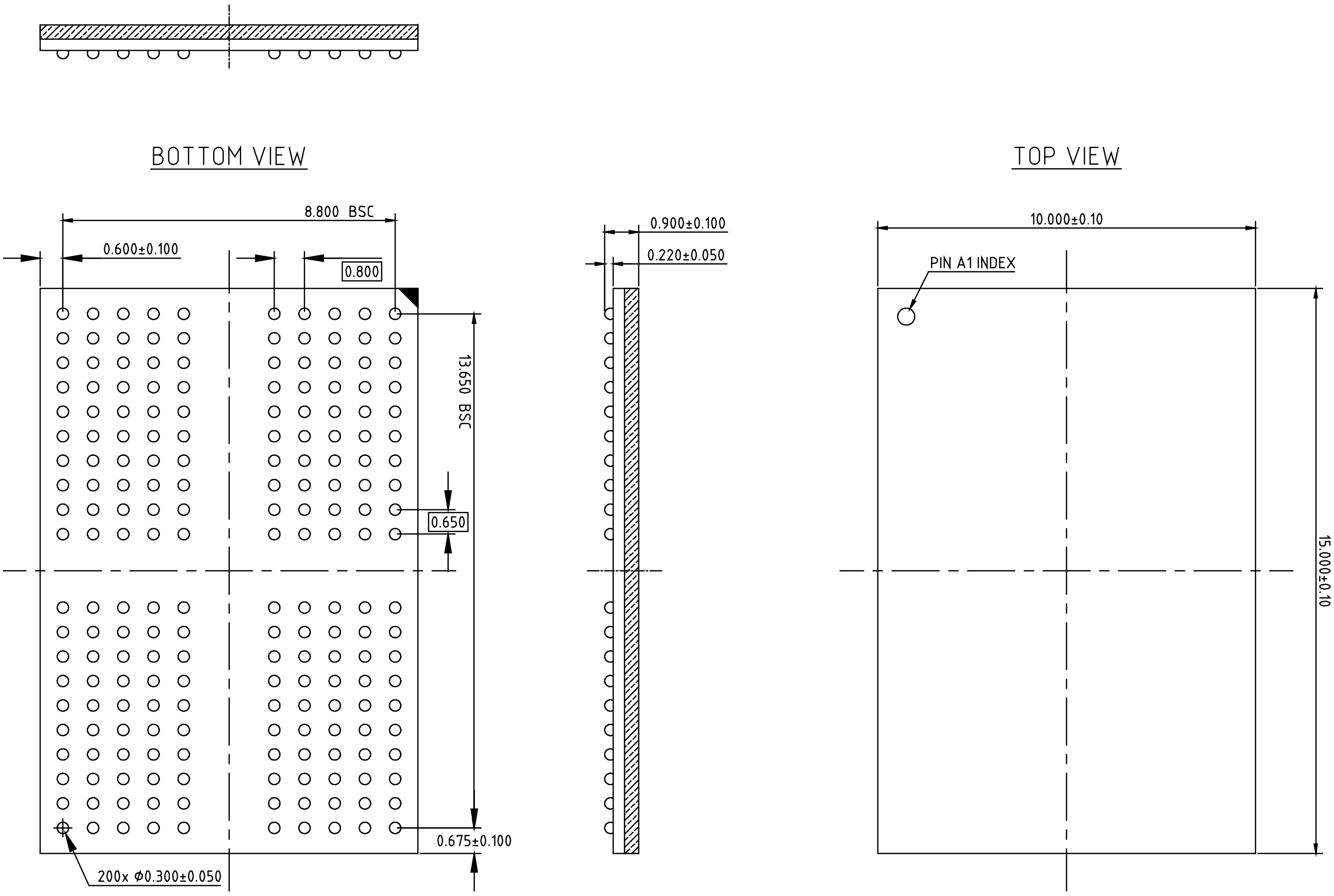
***UI = tCK(avg)min / 2**

Note:

1. Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply with the component Min-Max DC operating conditions.
2. The design specification is a BER < TBD. The BER will be characterized and extrapolated if necessary using a dual dirac method.
3. Rx mask voltage $V_{dIVW\_total(max)}$ must be centered around $V_{cent\_DQ(pin\_mid)}$.
4. V_{cent_DQ} must be within the adjustment range of the DQ internal V_{REF}.
5. DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. V_{IHL_AC} is the peak to peak voltage centered around $V_{cent\_DQ(pin\_mid)}$ such that V_{IHL_AC} /2 min must be met both above and below V_{cent_DQ}
6. DQ only minimum input pulse width defined at the $V_{cent\_DQ(pin\_mid)}$.
7. DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation.
8. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
9. TDQS2DQ max delay variation as a function of temperature.
10. TDQS2DQ max delay variation as a function of the DC voltage variation for V_{DDQ} and V_{DD2}. It includes the V_{DDQ} and V_{DD2} AC noise impact for frequencies > 20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package.
11. Input slew rate over V_{dIVW} Mask centered at $V_{cent\_DQ(pin\_mid)}$.
12. Rx mask defined for a one pin toggling with other DQ signals in a steady state.
13. V_{IHL_AC} does not have to be met when no transitions are occurring.
14. The same voltage and temperature are applied to tDQS2DQ_rank2rank.
15. tDQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
16. tDQS2DQ_rank2rank support was added to JESD209-4B, some older devices designed to support JESD209-4 and JESD209-4A may not support this parameter. Refer to vendor datasheet.

Package Diagram

200-Ball Fine Pitch Ball Grid Array Outline



Note: All dimensions are in millmeter.

Version History

Version	History	Date	Remarks
0.1	Preliminary Release	Aug, 2023	
0.2	1. Update the Addressing table 2. Update the Mode Register table	Aug, 2023	