Product Specification | Rev. 1.0 | 2025

IMM64M64D2DUS16AG (Die Revision D)
512MByte (64M x 64Bit)

512MB DDR2 Unbuffered DIMM
RoHS Compliant Product

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Features

- 240-Pin Unbuffered Dual-In-Line Memory Module
- JEDEC-Standard
- Capacity: 512MB
- 64Bit Data Bus Width without ECC
- Programmable CAS Latency (CL):
  - DDR2-800: 3, 4, 5
  - DDR2-667: 3, 4, 5
- Programmable Additive Latency (AL):
  - DDR2-800: 0, 1, 2, 3, 4
  - DDR2-667: 0, 1, 2, 3, 4
- Posted /CAS
- Write Latency (WL) = Read Latency (RL) - 1
- Power Supply: V_{DD}, V_{DDQ} = 1.8V ± 0.1V
- SSTL_18 Interface
- Bi-directional Differential Data-Strobe
  (Single-ended Data-Strobe is an optional feature)
- 8192 Refresh Cycle / 64ms
- Refresh Mode: Auto, Self
- Burst Type: Sequential, Interleave
- Burst Length: 8, 4
- On-Die Termination (ODT)
- Off-Chip Driver (OCD) Impedance Adjustment
- Serial Presence Detect (SPD) EEPROM
- Golde Edge Contacts
- 100% RoHS Compliant
- Standard Module Height: 30.00mm (1.18inch)

Table 1 - Ordering Information for RoHS Compliant Product

Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM64M64D2DUS16AG-Dzzzy(:qqq)	512MB	64Mx64	1	DDR2 Unbuffered DIMM

Note:

y:	Temperature Grade	(refer to Table 2)
zzz:	Speed Grade	(refer to Table 3)
qqq:	IM Reference Code	Blank or Reserved

Table 2 - Temperature Grade

Part Number	Temperature Grade	T_{CASE}
Blank	Commercial Temperature	0°C to 85°C
I	Industrial Temperature	-40°C to 95°C

Note: T_{CASE} is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to be double when 85°C < T_{CASE} ≤ 95°C

Table 3 - Speed Grade

Part Number	Speed Grade	Max. Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
25	DDR2-800	400MHz (2.5ns @ CL5)
3	DDR2-667	333MHz (3.0ns @ CL5)

Table 4 - Memory Chip Information

Part Number	Base Device Brand	Base Device	Voltage	Type	Chip Packing
IMM64M64D2DUS16AG-Dzzzy(:qqq)	IM	IM1G16D2DDBG	1.8V	64Mx16	Lead Free

Part Number Decoder

IM M 64M64 D2 DU S 16 A G - D 25 (I) (:qqq)

IM Module

DRAM Brand
M = IM

Module Configuration
64M64 = 64Mx64 (512MB)

Memory Type
D2 = DDR2

Module Form Factor
DU = Unbuffered DIMM (UDIMM)

Number of Rank
S = Single Rank

IM Reference code
Blank or Reserved

Temperature Grade
Blank = Commercial Temperature
(0℃ to +85℃ T_{CASE})
I = Industrial Temperature
(-40℃ to +95℃ T_{CASE})
***Note**: The refresh rate must be doubled when the operating temperature T_{CASE} exceeds +85℃*

Speed Grade
25 = DDR2-800 CL5

DRAM Revision
D = Revision D

Green Nature
G = RoHS Compliance

Module PCB Revision
A = Revision A

DRAM Bit Width
16 = using x16 components

Table 5 - Addressing

Parameter	512MB
Bank Address	8 BA[2:0]
Row Address	8K A[12:0]
Column Address	1K A[9:0]
Device Configuration	1Gb (64Mx16)
Module Rank Address	1 /S[0]_n
Number of Devices	4

Table 6 – Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{REF}	121	V_{SS}	61	A4	181	V_{DDQ}
2	V_{SS}	122	D4	62	V_{DDQ}	182	A3
3	D0	123	D5	63	A2	183	A1
4	D1	124	V_{SS}	64	V_{DD}	184	V_{DD}
5	V_{SS}	125	DM0	65	V_{SS}	185	CK0
6	/DQS0	126	NC	66	V_{SS}	186	/CK0
7	DQS0	127	V_{SS}	67	V_{DD}	187	V_{DD}
8	V_{SS}	128	D6	68	NC	188	A0
9	D2	129	D7	69	V_{DD}	189	V_{DD}
10	D3	130	V_{SS}	70	A10, AP	190	BA1
11	V_{SS}	131	D12	71	BA0	191	V_{DDQ}
12	D8	132	D13	72	V_{DDQ}	192	/RAS
13	D9	133	V_{SS}	73	/WE	193	/S0
14	V_{SS}	134	DM1	74	/CAS	194	V_{DDQ}
15	/DQS1	135	NC	75	V_{DDQ}	195	ODT0
16	DQS1	136	V_{SS}	76	/S1	196	A13
17	V_{SS}	137	CK1	77	ODT1	197	V_{DD}
18	NC	138	/CK1	78	V_{DDQ}	198	V_{SS}
19	NC	139	V_{SS}	79	V_{SS}	199	D36
20	V_{SS}	140	D14	80	D32	200	D37
21	D10	141	D15	81	D33	201	V_{SS}
22	D11	142	V_{SS}	82	V_{SS}	202	DM4
23	V_{SS}	143	D20	83	/DQS4	203	NC
24	D16	144	D21	84	DQS4	204	V_{SS}
25	D17	145	V_{SS}	85	V_{SS}	205	D38
26	V_{SS}	146	DM2	86	D34	206	D39
27	/DQS2	147	NC	87	D35	207	V_{SS}
28	DQS2	148	V_{SS}	88	V_{SS}	208	D44
29	V_{SS}	149	D22	89	D40	209	D45
30	D18	150	D23	90	D41	210	V_{SS}
31	D19	151	V_{SS}	91	V_{SS}	211	DM5
32	V_{SS}	152	D28	92	/DQS5	212	NC
33	D24	153	D29	93	DQS5	213	V_{SS}
34	D25	154	V_{SS}	94	V_{SS}	214	D46
35	V_{SS}	155	DM3	95	D42	215	D47
36	/DQS3	156	NC	96	D43	216	V_{SS}
37	DQS3	157	V_{SS}	97	V_{SS}	217	D52
38	V_{SS}	158	D30	98	D48	218	D53
39	D26	159	D31	99	D49	219	V_{SS}
40	D27	160	V_{SS}	100	V_{SS}	220	CK2
41	V_{SS}	161	NC	101	SA2	221	/CK2
42	NC	162	NC	102	NC	222	V_{SS}
43	NC	163	V_{SS}	103	V_{SS}	223	DM6
44	V_{SS}	164	NC	104	/DQS6	224	NC
45	NC	165	NC	105	DQS6	225	V_{SS}
46	NC	166	V_{SS}	106	V_{SS}	226	D54

Pin	Name	Pin	Name	Pin	Name	Pin	Name
47	V_{SS}	167	NC	107	D50	227	D55
48	NC	168	NC	108	D51	228	V_{SS}
49	NC	169	V_{SS}	109	V_{SS}	229	D60
50	V_{SS}	170	V_{DDQ}	110	D56	230	D61
51	V_{DDQ}	171	CKE1	111	D57	231	V_{SS}
52	CKE0	172	V_{DD}	112	V_{SS}	232	DM7
53	V_{DD}	173	A15	113	/DQS7	233	NC
54	BA2	174	A14	114	DQS7	234	V_{SS}
55	NC	175	V_{DDQ}	115	V_{SS}	235	D62
56	V_{DDQ}	176	A12	116	D58	236	D63
57	A11	177	A9	117	D59	237	V_{SS}
58	A7	178	V_{DD}	118	V_{SS}	238	V_{DDSPD}
59	V_{DD}	179	A8	119	SDA	239	SA0
60	A5	180	A6	120	SCL	240	SA1
58	A7	178	V_{DD}	118	V_{SS}	238	V_{DDSPD}
59	V_{DD}	179	A8	119	SDA	239	SA0
60	A5	180	A6	120	SCL	240	SA1

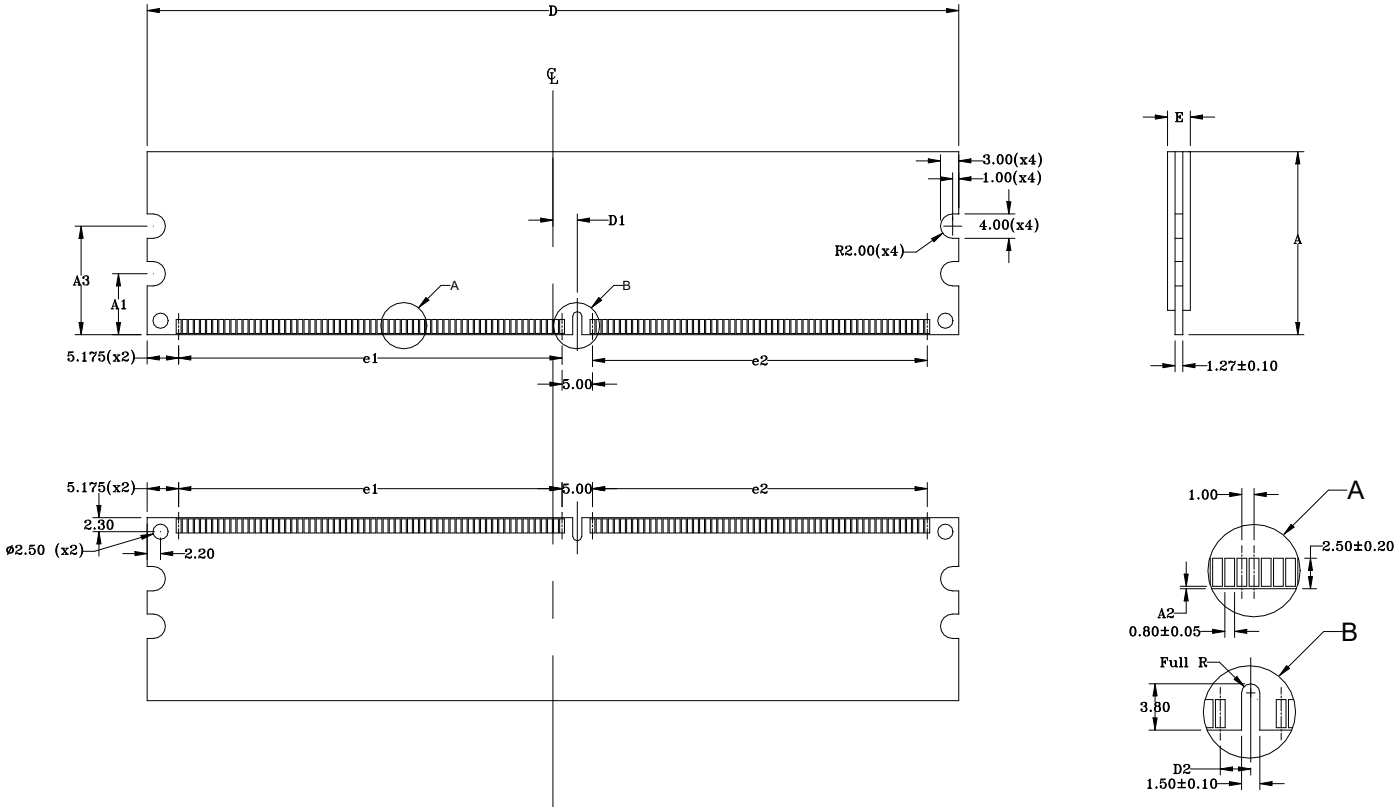
Note:
1. Pin 76, 77 and 171 are defined as NC for single rank module.

Table 7 - Pin Description

Pin Name	Description	Pin Name	Description
V_{DD}	SDRAM Core Power Supply	V_{DDQ}	SDRAM I/O Driver Power Supply
V_{REF}	SDRAM I/O Reference Supply	V_{SS}	Power Supply Return (Ground)
BA[2:0]	SDRAM Bank Address	A[15:0]	SDRAM Address Bus
/S[1:0]	DIMM Rank Chip Select	/RAS	SDRAM Row Address Strobe
/CAS	SDRAM Column Address Strobe	/WE	Write Enable
CKE[1:0]	SDRAM Clock Enable	ODT[1:0]	On-Die Termination Control Line
CK[2:0]	SDRAM Clock (Positive line of differential pair)	/CK[2:0]	SDRAM Clock (Negative line of differential pair)
D[63:0]	DIMM Memory Data Bus	DM[7:0]	SDRAM Data Mask
DQS[7:0]	SDRAM Data Strobe (Positive line of differential pair)	/DQS[7:0]	SDRAM Data Strobe (Negative line of differential pair)
V_{DDSPD}	Serial EEPROM Positive Power Supply	SCL	I^2C Serial Bus Clock for EEPROM
SA[2:0]	I^2C Slave Address Select for EEPROM	SDA	I^2C Serial Bus Data Line for EEPROM
NC	Spare Pin (No Connect)	-	-

Module Dimension

Figure 1 – 240 Pin DDR2 Unbuffered DIMM



Symbol	MIN	NOM	MAX
A	29.85	30.00	30.15
A1		10.00 BASIC	
A2	0.05	0.20	0.35
A3		17.80 BASIC	
D	133.20	133.35	133.50
D1		4.00 BASIC	
D2		2.50 BASIC	
e1		63.00 BASIC	
e2		55.00 BASIC	
E			4.00

Notes:
1. All dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. Tolerance on all dimensions is ±0.15 unless otherwise specified.
3. All dimensions are in millimeter.

Revision History

Revision	Descriptions	Release Date
1.0	Initial release	May, 2025